INSTALLATION MANUAL

AND TECHNICAL SPECIFICATIONS

OF THE MCX RANGE OF

COMMUNICATIONS CARDS

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I. INTRODUCTION

Thank you for purchasing an intelligent communications card from the MCX range.

The cards in this range are designed to be compatible with all systems built around a 16-bit EISA or ISA bus.

This documentation describes the installation procedure and the technical specifications for each of the cards in the range.

I.1 Presenting the MCX range

All the cards in the MCX range are designed around two basic models: the MCX-00 and the MCX-*Lite*/0. These cards along with their options and extensions meet a broad range of needs for serial communications.

These two models share the same architecture; the only difference concerns the extensions they support. This architecture is similar to that of a PC AT with a 386 microprocessor. Certain configurations can execute programs written for a PC on-card.

The MCX range is a series of intelligent communications cards. They have their own microprocessor (INTEL 80386SX 25 Mhz or CYRIX 486SLC at 25 Mhz, Texas Instruments 486 SXLC2 50 Mhz) to manage the communications channels.

Each card has 2 Mbytes of RAM which may be expanded up to 16 Mbytes, a hardware "watchdog", a keyboard controller and a 256 Kbyte FLASH EPROM containing a PC-compatible BIOS.

The card and the host can use three means to communicate :
- The host computer can access any location of the MCX RAM through a 32Kbyte dual-ported Window. The card manages all conflicts. It automatically adapts to the host machine's bus speed.
- The host computer and the board can send interrupts to each other.
- The card can use a 256-byte FIFO to send data to the host.

I.1.1 The MCX-00 card

This basic model, when associated with one or more MCX-BP extensions, can control up to 64 synchronous or asynchronous RS232D or RS422A serial ports. As of 16 lines (2 MCX-BP units) in RS422A or 24 lines (3 MCX-BP units) in RS232D, an additional power supply (MCX-PWS) is required.

An MCX-08 is an MCX-00 with an MCX-BP extension (8 channels); an MCX-16 is an MCX-00 with two MCX-BP extensions, and so forth.

The MCX-00 supports the following options and extensions:

- MCX-486 .....486 SLC 25Mhz, 486 SXLC2 50 Mhz.
- MCX-387 .....80387 25 Mhz arithmetic coprocessor.
- MCX-RAM .....Additional RAM.
- MCX-BP .....8 channel synchronous or asynchronous RS232D or RS422A unit with an SCC 85C30.
- MCX-BP85230 .....8 channel synchronous or asynchronous RS232D or RS422A unit with an SCC 85230.
- MCX-CABLE .....Cable to connect an MCX-BP unit to the MCX-00 card.
- MCX-PWS .....Additional power supply for the MCX-16 card and above.
- MCX-PCMCIA .....Extension kit for connection PCMCIA 2.0 cards.
- MCX-MODEM/0.....Empty housing with connections for interface cards.
- MCX-MH.....V32bis modem card for the MCX-MODEM/0.
- MCX-MH8.....Unit with 8 MCX-MH modems.
- MCX-SLOT .....Kit for attaching 2 AT 16 bit cards to the MCX-00.
- MCX-RACK 19″.....External 19″3U rack with power supply for mounting an MCX-00 card in stand-alone mode.

I.1.2 The MCX-*Lite*/0 card

The MCX-*Lite*/0 card is compatible with the MCX-00 card.

This model supports the following options and extensions:

- MCX-486 .....486 SLC 25Mhz, 486 SXLC2 50 Mhz.
- MCX-RAM .....Additional RAM.
- *Lite*-SERIAL extension....2 synchronous or asynchronous RS232D or RS422A serial channels (SCC 85C30).
- *Lite*-UNX extension .....4 or 8 asynchronous RS232D or RS422A serial channels (16C550 UARTs).
- *Lite*-485 extension.....2 asynchronous RS232D, RS422A, RS485 isolated serial channels, or in current loop (16C550 UARTs) + 1 parallel port.
- *Lite*-104 extension.....1 asynchronous RS232D, RS422A, RS485 serial channel, not isolated and the connections to attach 2 PC-104 cards.

When attached to the *Lite*-104 extension, the assembly is called the MCX-*Lite*/104 card.

When attached to the *Lite*-485 extension, the assembly is called the MCX-*Lite*/485 card.

When attached to the *Lite*-SERIAL extension, the assembly is called the MCX-*Lite*/S card, the equivalent of one-quarter of an MCX-08.

When attached to the *Lite*-UNX, you obtain the equivalent of the MCX-*Lite*/U card.
The *Lite*-UNX was designed to be compatible with DOS applications that use traditional, dumb communications cards. The MCX-*Lite*/U card functions just like a PC with an ACKSYS UNX232-550 communications card. Any DOS program that uses the UNX232 can be run with no modifications on the MCX-*Lite*/U card. All the options of the UNX232 card are compatible with the *Lite*-UNX extension (UNXBP+, BC20MA-UNX, AD422-485-UNX).

Unlike the MCX-00 card, the MCX-*Lite*/0 card has no keyboard connector, nor a socket for the MCX-387 extension.

I.2 Programming modes

Each type of card offers several programming options, summarized in the following paragraphs.

I.2.1 Using the ACKSYS programs in the FLASH EPROMs

Two ACKSYS programs contained in the FLASH EPROM help the programmer manage the card's 2 to 64 channels:

- The basic program, delivered with all cards, for asynchronous communications only.
- The optional multiprotocol program also manages certain synchronous protocols.

This mode is only available on MCX cards with SCC 85C30-type communication devices.

ACKSYS provides the system-level software drivers[1] to let programmers carry out low-level communications with the card.

If the ACKSYS driver is installed, the PC application accesses the communication lines as if they were files. It can then use standard operating system functions (system calls such as READ, WRITE, IOCTL, etc.).

If the driver is not installed, the application can use the card without operating system limitations, but it is up to the application to manage access to the card.

Applications to be developed	Applications resident on the card	Applications resident on the PC
Use the PC to develop the application to run on the PC using the development environment of your choice under: - DOS, Windows, UNIX, - OS/2 etc.	Basic program or Optional multiprotocol program	Your application + ACKSYS driver or Your application alone

[1] Contact ACYSYS for driver availability.

I.2.2 Developing custom applications with MCXDEBUG

MCXDEBUG is available on MCX cards equipped with SCC 85C30 communication devices.

MCXDEBUG is a platform for developing MCX applications under DOS, offering:

- A debugging system (MCXDEBUG).
- A library (MCXLIB).
- A program loader for MCS-86 format programs (MCXLOAD[2]).

Applications to be developed	Applications resident on the card	Applications resident on the PC
Use the PC to develop applications designed to run on the card, and download the program to the card using MCXLOAD. Use the PC to develop the application designed to run on the host PC.	Your application	Your application

[2] MCXLOAD also exists for SCO UNIX, INTERACTIVE 386/IX and QNX.

I.2.3 Developing custom applications with MCXDOS

MCXDOS exploits the PC structure of the MCX card. It is a resident DOS program that acts like a shared network server.

It is loaded after the operating system and lets you load MS-DOS both in your machine and in the MCX card.
The MCXDOS program lets you share your machine's resources (disk drive, monitor, keyboard, mouse) with the MCX card.

You can develop an application at the same time on your machine and on the MCX card; you switch the PC resources to the MCX using a keystroke combination.
You can quickly and easily switch from the virtual MCX machine to your PC.

This makes it very easy to develop applications for the MCX card because you use exactly the same compilers and development tools that you are familiar with on your PC.

MCXDOS is delivered with a library of routines to access MCX peripherals that are not in the standard PC structure.

Applications to be developed	Applications resident on the card	Applications resident on the PC
Use the card to develop the application designed to run on the card. Use the PC to develop the application designed to run on the PC.	Your application + MS-DOS + MCXDOS program	Your application + MS-DOS, WINDOWS 3.1, WINDOWS 95 + MCXDOS program

I.3 Warranty

The warranty period is specified in our terms of sale:

a 5 year warranty on parts[1] and labor against any manufacturing defects except for failures due to non-standard usage or by excessive actions of a third party or natural circumstances.

Repairs under warranty shall be performed on our premises, in a maximum of two working days.

NOTICE

Electrical current from the power supply, the telephone and transmission cables may be dangerous.

- Only connect and disconnect cables when the host machine for your card is powered off.
- Do not touch the cables during storms.

D A N G E R

NEVER CONNECT OR DISCONNECT THE SUB D CONNECTORS WHEN THE MACHINE IS POWERED ON.

Failures are often due to repeated manipulation of the RS232D connectors on the SUB D25 and/or the SUB D9 connectors when the machine is powered on. They usually destroy the line amplifiers in the connection device.

Most failures can easily be avoided by following the recommendation above.

PLEASE FOLLOW THIS ADVICE !

[1] Except for the lithium battery.

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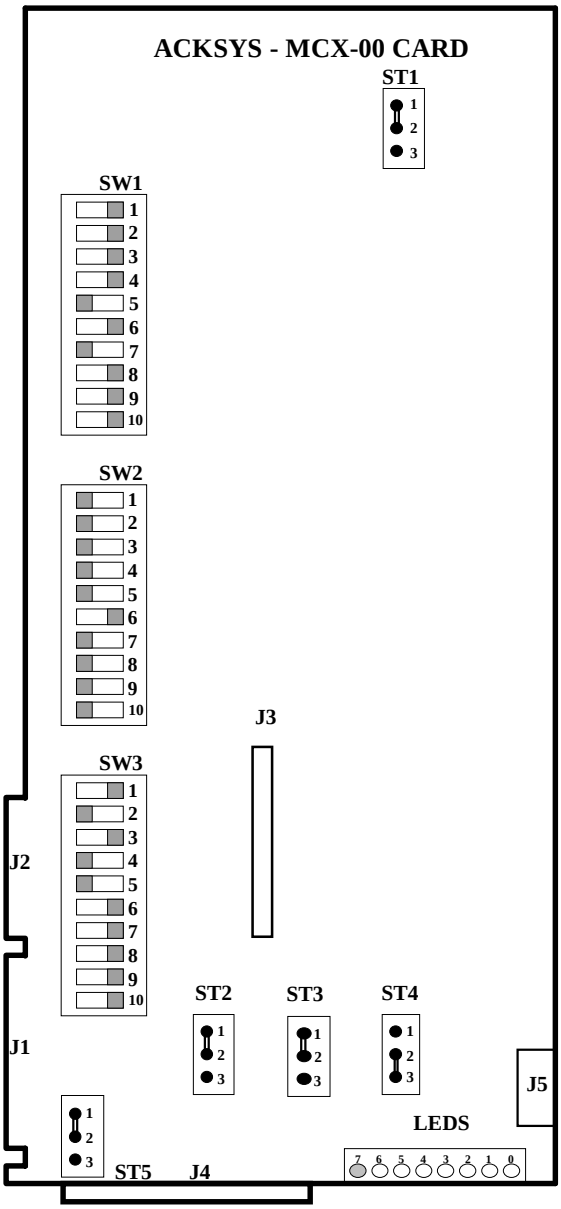
II. THE MCX-00 CARD

II.1 Installing the card

The card must be installed in a 16-bit slot.

II.1.1 Jumpers and switch settings



Factory settings	SW1 = 280h SW2 = IRQ10 SW3 = D000h ST1 on 1-2, ST2 on 1-2, ST3 on 1-2, ST4 on 2-3 et ST5 on 1-2

II.1.2 Selecting the interrupt level

The DIP switches at SW2 let you select one of ten interrupt levels.

Before selecting an interrupt level, make sure it is not already used by another peripheral already installed in your machine.

Once you have chosen the interrupt, use the table below to select the combination desired:

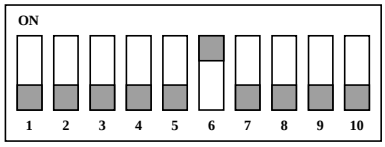
sw2-1	sw2-2	sw2-3	sw2-4	sw2-5	sw2-6	sw2-7	sw2-8	sw2-9	sw2-10
IRQ9	IRQ3	IRQ4	IRQ5	IRQ7	IRQ10	IRQ11	IRQ12	IRQ14	IRQ15

DIP switch SW2 - Selecting the interrupt level

To select an interrupt level, simply move the switch corresponding to your choice to the "ON" position.

Warning: you cannot select two levels at once. All other switches must be in the "OFF" position.

Note:
The "ON" position means the switch is pushed up.



Default interrupt: SW2-6 = IRQ10

When delivered from the factory, the IRQ10 interrupt is selected.

II.1.3 Selecting the base address

The address of the card's dual-ported memory may be selected in the memory space between 512 Kbytes and 16 Mbytes using a set of 10 switches (SW3).

The card occupies a contiguous block of 32 Kbytes of memory.

Before selecting the card's address in memory, make sure the address is available, and that any cache memory does not cover this area with system memory.

The table below indicates the address bits associated with the different switches:

sw3-1	sw3-2	sw3-3	sw3-4	sw3-5	sw3-6	sw3-7	sw3-8	sw3-9	sw3-10
A15	A16	A17	A18	A19	A20	A21	A22	A23	N/A

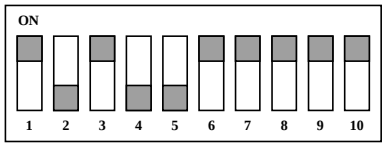
Inter DIL SW3 - Selecting the memory address[1]

The example below illustrates how to encode an address:

A23	A22	A21	A20	A19	A18	A17	A16	A15
0	0	0	0	1	1	0	1	0

or 0 D 0

This corresponds to:



Address: 0D0000h

Note:
The "ON" position means the switch is pushed up. The switch must be OFF to enable the address bit at 1.

When delivered from the factory, the selected base address is 0D0000h.

[1] The appendix entitled "Configuring the SW3 switch" provides the most common configurations for SW3.

II.1.4 Selecting the input/output address

The PC communicates with the board using a group of eight I/O addresses. You can define the base address using the block of 10 switches at SW1. The card's base I/O address may be selected in the PC's I/O address space between 0 and 1FFFh.

Note that most PCs do not decode I/O addresses beyond 400h, or 800h, depending on the manufacturer. If you choose 800h as your base address, it is very likely that your card will be decoded at address 0, which will prevent your system from operating correctly.

The table below illustrates the address bits associated with the various switches:

sw1-1	sw1-2	sw1-3	sw1-4	sw1-5	sw1-6	sw1-7	sw1-8	sw1-9	sw1-10
A3	A4	A5	A6	A7	A8	A9	A10	A11	A12

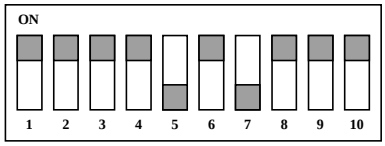
DIP switch SW1 - Selecting the I/O address

The example below illustrates how to encode an address on SW1:

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
0	0	0	1	0	1	0	0	0	0
or 0			2			8			0

Note:
The "ON" position means the switch is pushed up. The switch must be OFF to enable the address bit at 1.

This corresponds to:



Address: 0280h

When delivered from the factory, the cards are encoded at an I/O address of 280h and therefore occupy the I/O addresses between 280h and 287h.

II.1.5 Jumper settings

The card has **five jumpers** which let you configure its operating mode.

- **ST1**
  The ST1 jumper controls the card's built-in "watchdog" functions.

  - ST1 on 1-2: Enables the "watchdog". It can be controlled by software.
  - ST1 on 2-3: Disables the "watchdog".

- **ST2 and ST3**
  These two jumpers control some of the card's software functions.

  - ST2 on 1-2 and ST3 on 1-2: This is the card's default setting. This combination enables the MCC emulation mode (enables the asynchronous command interpreter or the multiprotocol command interpreter); this mode lets you use MCXDEBUG.
  - ST2 on 2-3 and ST3 on 1-2: This setting enables the card's PC compatible mode. In this mode you can use the MCX-00 card in "stand-alone" mode with the MCX-SLOT extension which provides 2 ISA expansion slots, or with the PCMCIA extension.
  - ST2 on 1-2 and ST3 on 2-3: Reserved for ACKSYS.
  - ST2 on 2-3 and ST3 on 2-3: This combination lets you use the MCX-DOS software.

- **ST4**
  The ST4 jumper lets you connect the +12V FLASH required to program the 256 Kbytes of FLASH memory.

  - ST4 on 1-2: You may dynamically program the FLASH memory (the FLASH command).
  - ST4 on 2-3: The programming pin is set to +5V to prevent any accidental programming.

- **ST5 (Revision B and later)**
  The ST5 jumper controls the RESET signal sent by the PC system.

  - ST5 on 1-2: A RESET performed on the PC will be sent to the card.
  - ST5 on 2-3: A RESET performed on the PC will not effect the card.

When delivered from the factory, the jumpers are configured as follows:
ST1 on 1-2, ST2 on 1-2, ST3 on 1-2, ST4 on 2-3 and ST5 on 1-2

II.2 Electrical and mechanical specifications

POWER CONSUMPTION	DIMENSIONS	OPERATING CONDITIONS		
+ 5 V DC	Length x Width	Relative humidity (not condensed)	Temperature	Storage
1.60 A max / 8 W	340mm x 115mm	95% at +25°C	from -5 to +65°C	from -25 to +70°C

The dimensions do not include the J4 connector, the attachment bar and the 2 ISA connectors. Power consumption calculations are based on an MCX-00 card with an 80386SX 25 Mhz processor, an 80387SX 25 Mhz coprocessor and 4 Mbytes RAM.

II.2.1 Connector descriptions

- **J3 Connector**
  You may attach the following extensions to this connector:
  - MCX-SLOT (lets the card operate in "stand-alone" mode)
  - MCX-PCMCIA (lets you connect a PCMCIA 2.0 card)

- **J4 Connector**
  This connector, accessible from outside the PC, lets you connect the first extension unit (MCX-BP or MCX-MODEM/0) to the MCX-00 card using the MCX-CABLE supplied.

- **J5 Connector**
  This lets you connect a keyboard to the card in MCXDOS or "stand-alone" mode.

II.3 Programming

This information is provided only for writing programs that are internal to the card.

II.3.1 Input/Output ports on the MCX-00 card

This section provides an exhaustive list of the I/O ports on the MCX-00 card.

* **Address 80h - Control the display of the group of 8 LEDs - (Write only):**

D0 ..... LED 0
D1 ..... LED 1
D2 ..... LED 2
D3 ..... LED 3
D4 ..... LED 4
D5 ..... LED 5
D6 ..... LED 6
D7 ..... LED 7 (red LED)

Setting a bit to 1 turns on the corresponding LED.

* **Address 500h - Trigger an interrupt on the host PC - (Write only):**

D0 set to 0 ..... disables the interrupt line
D0 set to 1 ..... enables the interrupt line

This interrupt line may be physically attached to the following IRQ lines in the host PC: IRQ9 (or IRQ2), IRQ3, IRQ4, IRQ5, IRQ7, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15; use the SW2 switch to select the interrupt (positions 1 to 10 respectively).

* **Address 501h - Potential PPV used by the FLASH memory - (Write only):**

D0 set to 0 ..... PPV = +5V Read Flash mode
D0 set to 1 ..... PPV = +12V programming mode

* **Address 503h - Clear Interrupt (IRQ9) coming from the PC - (Write only):**

D0 set to 0 or 1 ..... removes the interrupt generated by the PC

The interrupt generated by the PC is physically connected to the IRQ9 interrupt line on the MCX card.

*** Address 504h - Status / Control Register - (Read/Write):**

When reading:

D0 ..... /Fifo Full Bit (from MOSEL 7200):
Also indicates the status of the MCX card's IRQ10 interrupt line.

D1 ..... /Fifo Not Empty Bit (from MOSEL 7200):
Indicates the same status as the interrupt line selected on the PC when using the FIFO buffer.
0 = INT idle
1 = INT active

D2 ..... /Fifo Half Full Bit (from MOSEL 7200).

D3..... Indicates the status of the interrupt line selected on the PC whether or not the FIFO buffer is used.
0 = INT idle
1 = INT active

D4 ..... Indicates the position of the jumper at ST3
0 = position 2-3
1 = position 1-2

D5 ..... Indicates the position of the jumper at ST2
0 = position 2-3
1 = position 1-2

D6 ..... POWER FAIL Bit:
0 = power supply failure on the MCX card.

D7 ..... BAT-LOW Bit:
set to 0, indicates that the Lithium battery should be replaced. Reading this bit is only valid if the BAT-TEST bit has first been set to 0 (Address 504h when writing, least significant bit).

When writing:

D0 ..... BAT-TEST Bit:
when set to 0, enables reading the BAT-LOW bit (as described above).

D1 ..... INT-MBX-ENABLE Bit:
Controls the dual-ported memory interrupt. When set to 1, this bit enables the interrupts generated by the PC when writing to addresses 0 or 1 of the dual-ported memory. These interrupts are received on the MCX card's IRQ9 line. When set to 0, this bit disables this type of interrupt.

D2 ..... This bit controls the delay for triggering the "Watchdog".
If D2=1, this delay is 1.6 seconds; it is 100 ms if D2 = 0.

D3 ..... Initial window address (A15).
D4 ..... Initial window address (A16).
D5 ..... Initial window address (A17).
D6 ..... Initial window address (A18).
D7 ..... Initial window address (A19).
These bits define the address of the 32 Kbyte initial logical memory page as seen by the PC. The other address bits A20, A21, A22 and A23 are forced to 0 during this operation.

Warning: Writing to this register for the first time automatically validates the Bus Master mode for PC access towards the MCX card. You must have set channel 0 of DMA controller number 1 to cascade mode before writing to this register.
If you access this register before initializing the Bus Master mode, all PC access to the dual-ported memory will be blocked (as well as the PC!).
You should also note that this logical page is only valid until the host PC sets another page.

* **Address 505h - Restart the "Watchdog" - (Write only):**

D0 set to 0 or 1 ..... Restarts (refreshes) the "Watchdog" timer.

* **Address 506h - Control the "Watchdog" - (Write only):**

D0 set to 0 ..... "watchdog" disabled.
D0 set to 1 ..... "watchdog" enabled.

The "watchdog" may still be disabled by ST1. If the jumper at ST1 is set to position 2-3, the "watchdog" is disabled, whatever the contents of the control register. In position 1-2, however, the "watchdog" may be enabled and disabled according to the contents of the control register.

* **Address 507h - FIFO / PAGE - (Read/Write):**

When reading:

When reading, bits D0 to D7 indicate which 32 Kbyte page has been selected by the PC as dual-ported memory.
Bits D0 to D7 have the following meaning:

D0 ..... Window address (A15)
D1 ..... Window address (A16)
D2 ..... Window address (A17)
D3 ..... Window address (A18)
D4 ..... Window address (A19)
D5 ..... Window address (A20)
D6 ..... Window address (A21)
D7 ..... Window address (A22)

Address bit A23 is always hard-wired to 0 on the MCX card.

1st MEGABYTE				2nd MEGABYTE	
Window address (Hex)	**PAGE register (Hex)**	**Window address (Hex)**	**PAGE register (Hex)**	**Window address (Hex)**	**PAGE register (Hex)**
00000	00	80000	10	100000	20
08000	01	88000	11	108000	21
10000	02	90000	12	110000	22
18000	03	98000	13	118000	23
20000	04	A0000	14	120000	24
28000	05	A8000	15	128000	25
30000	06	B0000	16	130000	26
38000	07	B8000	17	138000	27
40000	08	C0000	18	140000	28
48000	09	C8000	19	148000	29
50000	0A	D0000	1A	150000	2A
58000	0B	D8000	1B	158000	2B
60000	0C	E0000	1C	160000	2C
68000	0D	E8000	1D	168000	2D
70000	0E	F0000	1E	170000	2E
78000	0F	F8000	1F	178000	2F

Excerpt of the correspondence table between window addresses and the Page register.

When writing:

When writing, port 507h lets you write to the FIFO register, which may contain 256 bytes.

II.3.2 Input/output ports on the host PC

The base input/output (I/O) address of the MCX card for the host PC is set by the DIL SW1 switch. The factory setting for the base I/O address is 280h.

* **Address Base + 0 - Read FIFO - (Read only):**

  This I/O port lets you read the contents of the FIFO buffer which was previously filled by the MCX card (this FIFO buffer is 256 bytes deep). If the buffer is empty the value obtained is 0FFH (255).

* **Address Base + 0 - RESET MCX - (Write only):**

  This I/O port lets you "reset" the MCX card. This reset occurs 1.6 seconds after writing to this address. This feature is only available on REV C cards and later, with the Watchdog jumper set (ST1 in position 1-2). Warning: Validating the watchdog by software has no effect.

* **Address Base + 1 - Write PAGE - (Write only):**

  Bits D0 to D7 let you select a logical 32 Kbyte page in the memory of the MCX card that will be accessible in the PC window.

  D0 ..... Logical page address- A15.
  D1 ..... Logical page address- A16.
  D2 ..... Logical page address- A17.
  D3 ..... Logical page address- A18.
  D4 ..... Logical page address- A19.
  D5 ..... Logical page address- A20.
  D6 ..... Logical page address- A21.
  D7 ..... Logical page address- A22.

  Address bit A23 is hard-wired to 0 on the MCX card. Warning: Writing to this register the first time disables the page selection performed by the MCX card during its initialization.

* **Address Base + 2 - PC TO MCX INT - (Write only):**

  Writing to this address triggers an interrupt to the MCX card (IRQ9 line on the card). This is an alternate method for waking up the MCX card at the interrupt generated when writing to addresses 0 and 1 in the dual-ported memory.
  The contents of the data bits is not significant.

*** Address Base + 3 - Clear MCX TO PC INT:**

When writing:

Writing to this address resets the interrupt generated by the MCX and destined for the host PC. The contents of the data bits are not significant.

When reading: (MCX-00 Rev B and later)

Reading this register returns the following information:

D0..... MCX-TO-PC-INT Bit:
when set to 0, this bit indicates that the interrupt signal generated by the MCX card (D-Type Flip-Flop address 500H) is idle. When the signal is active this bit equals 1.

D1..... FIFO-EMPTY Bit:
set to 0, it indicates that the FIFO buffer is empty; set to 1, it indicates that the FIFO buffer contains at least one byte.

D2..... MCX-INT Bit:
set to 1, it indicates that the MCX card has not yet disabled the interrupt generated by the PC.

D3..... WIN-SET Bit:
set to 0, this bit indicates that the MCX card has set its initial logical page and that the data read in the PC window is valid. Set to 1, it indicates that this operation has not yet taken place, or that the host PC has selected a new logical page in the window.

D4..... ST2 Bit:
set to 1, it indicates that the ST2 jumper on the MCX card is in position 1-2; set to 0, the jumper is in 2-3.

D5..... ST3 Bit:
set to 1, it indicates that the ST3 jumper on the MCX card is in position 1-2; set to 0, the jumper is in 2-3.

Bits D6 and D7 are not significant.

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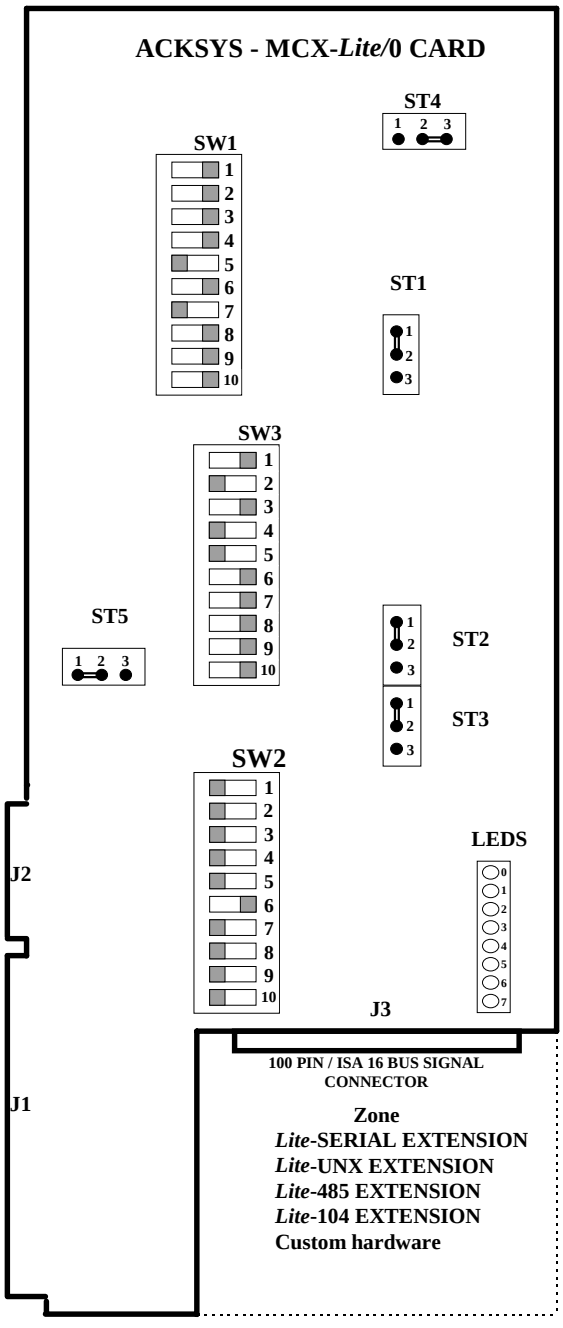
III. THE MCX-*LITE*/0 CARD

III.1 Installing the card

The card must be installed in a 16-bit slot.

III.1.1 Jumpers and switch settings



Factory settings	SW1 = 280h SW2 = IRQ10 SW3 = D000h ST1 on 1-2, ST2 on 1-2, ST3 on 1-2, ST4 on 2-3 et ST5 on 1-2

III.1.2 Selecting the interrupt level

The DIP switches at SW2 let you select one of ten interrupt levels.

Before selecting an interrupt level, make sure it is not already used by another peripheral already installed in your machine.

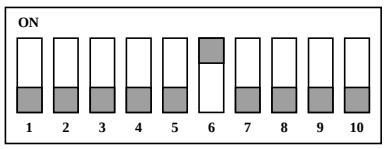
Once you have chosen the interrupt, use the table below to select the combination desired:

sw2-1	sw2-2	sw2-3	sw2-4	sw2-5	sw2-6	sw2-7	sw2-8	sw2-9	sw2-10
IRQ9	IRQ3	IRQ4	IRQ5	IRQ7	IRQ10	IRQ11	IRQ12	IRQ14	IRQ15

DIP switch SW2 - Selecting the interrupt level

To select an interrupt level, simply move the switch corresponding to your choice to the "ON" position.
Warning: you cannot select two levels at once. All other switches must be in the "OFF" position.

Note:
The "ON" position means the switch is pushed up.



Default interrupt: SW2-6 = IRQ10

When delivered from the factory, the IRQ10 interrupt is selected.

III.1.3 Selecting the base address

The address of the card's dual-ported memory may be selected in the memory space between 512 Kbytes and 16 Mbytes using a set of 10 switches (SW3).

The card occupies a contiguous block of 32 Kbytes of memory.

Before selecting the card's address in memory, make sure the address is available, and that any cache memory does not cover this area with system memory.

The table below indicates the address bits associated with the different switches:

sw3-1	sw3-2	sw3-3	sw3-4	sw3-5	sw3-6	sw3-7	sw3-8	sw3-9	sw3-10
A15	A16	A17	A18	A19	A20	A21	A22	A23	N/A

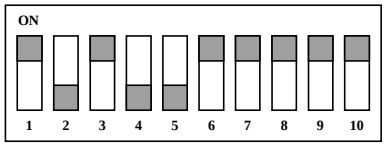
DIP switch SW3 - Selecting the memory address[1]

The example below illustrates how to encode an address:

A23	A22	A21	A20	A19	A18	A17	A16	A15
0	0	0	0	1	1	0	1	0

or 0 D 0

This corresponds to:



Address: 0D0000h

Note:
The "ON" position means the switch is pushed up. The switch must be OFF to enable the address bit at 1.

When delivered from the factory, the selected base address is 0D0000h.

[1] The appendix entitled "Configuring the SW3 switch" provides the most common configurations for SW3.

III.1.4 Selecting the input/output address

The PC communicates with the board using a group of eight I/O addresses. You can define the base address using the block of 10 switches at SW1. The card's base I/O address may be selected in the PC's I/O address space between 0 and 1FFFh.

Note that most PCs do not decode I/O addresses beyond 400h, or 800h, depending on the manufacturer. If you choose 800h as your base address; it is very likely that your card will be decoded at address 0, which will prevent your system from operating correctly.

The table below illustrates the address bits associated with the various switches:

sw1-1	sw1-2	sw1-3	sw1-4	sw1-5	sw1-6	sw1-7	sw1-8	sw1-9	sw1-10
A3	A4	A5	A6	A7	A8	A9	A10	A11	A12

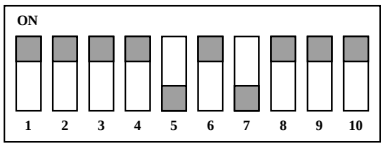
DIP switch SW1 - Selecting the I/O address

The example below illustrates how to encode an address on SW1:

	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
	0	0	0	1	0	1	0	0	0	0
or	0			2			8			0

Note:
The "ON" position means the switch is pushed to the top. The switch must be OFF to enable the address bit at 1.

This corresponds to:



Address: 0280h

When delivered from the factory, the cards are encoded at an I/O address of 280h and therefore occupy the I/O addresses between 280h and 287h.

III.1.5 Jumper settings

The card has **five jumpers** which let you configure its operating mode.

- **ST1**
  The ST1 jumper controls the card's built-in "watchdog" functions.

  - ST1 on 1-2: Enables the "watchdog". It can be controlled by software.
  - ST1 on 2-3: Disables the "watchdog".

- **ST2 and ST3**
  These two jumpers control some of the card's software functions.

  - ST2 on 1-2 and ST3 on 1-2: This is the card's default setting. This combination enables the MCC emulation mode (enables the asynchronous command interpreter or the multiprotocol command interpreter); this mode lets you use MCXDEBUG.
  - ST2 on 2-3 and ST3 on 1-2: This setting enables the card's PC compatible mode. In this mode you can use the MCX-*Lite/*0 card in "stand-alone" mode with the Lite-104 extension.
  - ST2 on 1-2 and ST3 on 2-3: Reserved for ACKSYS.
  - ST2 on 2-3 and ST3 on 2-3: This combination lets you use the MCX-DOS software.

- **ST4**
  The ST4 jumper lets you connect the +12V FLASH required to program the 256 Kbytes of FLASH memory.

  - ST4 on 1-2: You may dynamically program the FLASH memory (the FLASH command).
  - ST4 on 2-3: The programming pin is set to +5V to prevent any accidental programming.

- **ST5 (Revision B and later)**
  The ST5 jumper controls the RESET signal sent by the PC system.

  - ST5 on 1-2: A RESET performed on the PC will be sent to the card.
  - ST5 on 2-3: A RESET performed on the PC will not affect the card.

When delivered from the factory, the jumpers are configured as follows:
ST1 on 1-2, ST2 on 1-2, ST3 on 1-2, ST4 on 2-3 and ST5 on 1-2

III.2 Electrical and mechanical specifications

POWER CONSUMPTION	DIMENSIONS	OPERATING CONDITIONS		
+ 5 V DC	Length x Width	Relative humidity (not condensed)	Temperature	Temperature
1.48 A max / 7.4 W	340mm x 115mm	95% at +25°C	from -5 to +65°C	from -25 to +70°C

The dimensions do not include the ISA connectors.

Power consumption calculations are based on an MCX-*Lite*/0 card with an 80386SX 25 Mhz processor and 4 Mbytes RAM.

III.2.1 Connector descriptions

- **J3 ISA 100 pin connector**
  The following extensions may be attached to this connector:
  - *Lite*-SERIAL,
  - *Lite*-UNX,
  - *Lite*-485,
  - *Lite*-104,
  - Custom hardware.

III.3 Programming

This information is provided only for writing programs that are internal to the card.

III.3.1 Input/Output ports on the MCX-*Lite*/0 card

This section provides an exhaustive list of the I/O ports on the MCX-*Lite*/0 card.

* **Address 80h - Control the display of the group of 8 LEDs - (Write only):**

D0 ..... LED 0
D1 ..... LED 1
D2 ..... LED 2
D3 ..... LED 3
D4 ..... LED 4
D5 ..... LED 5
D6 ..... LED 6
D7 ..... LED 7 (red LED)

Setting a bit to 1 turns on the corresponding LED.

* **Address 500h - Trigger an interrupt on the host PC - (Write only):**

D0 set to 0 ..... disables the interrupt line
D0 set to 1 ..... enables the interrupt line

This interrupt line may be physically attached to the following IRQ lines in the host PC: IRQ9 (or IRQ2), IRQ3, IRQ4, IRQ5, IRQ7, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15; use the SW2 switch to select the interrupt (positions 1 to 10 respectively).

* **Address 501h - Potential PPV used by the FLASH memory - (Write only):**

D0 set to 0 ..... PPV = +5V Read Flash mode
D0 set to 1 ..... PPV = +12V programming mode

* **Address 503h - Clear interrupt (IRQ9) coming from the PC - (Write only):**

D0 set to 0 or 1 ..... removess the interrupt generated by the PC.

The interrupt generated by the PC is physically connected to the IRQ9 interrupt line on the MCX-*Lite*/0 card.

*** Address 504h - Status / Control Register - (Read/Write):**

When reading:

D0 ..... /Fifo Full Bit (from MOSEL 7200):
Also indicates the status of the MCX-*Lite*/0 card's IRQ10 interrupt line.

D1 ..... /Fifo Not Empty Bit (from MOSEL 7200):
Indicates the same status as the interrupt line selected on the PC when using the FIFO buffer.
0 = INT idle
1 = INT active

D2 ..... /Fifo Half Full Bit (from MOSEL 7200).

D3..... Indicates the status of the interrupt line selected on the PC whether or not the FIFO buffer is used.
0 = INT idle
1 = INT active

D4 ..... Indicates the position of the jumper at ST3
0 = position 2-3
1 = position 1-2

D5 ..... Indicates the position of the jumper at ST2
0 = position 2-3
1 = position 1-2

D6 ..... POWER FAIL Bit:
0 = power supply failure on the MCX-*Lite*/0 card.

D7 ..... BAT-LOW Bit:
set to 0, indicates that the Lithium battery should be replaced. Reading this bit is only valid if the BAT-TEST bit has first been set to 0 (Address 504h when writing, least significant bit).

When writing:

D0 ..... BAT-TEST Bit:
when set to 0, enables reading the BAT-LOW bit (as described above).

D1 ..... Controls the dual-ported memory interrupt. When set to 1, this bit enables the interrupts generated by the PC when writing to addresses 0 or 1 of the dual-ported memory. These interrupts are received on the MCX-*Lite/*0 card's IRQ9 line. When set to 0, this bit disables this type of interrupt.

D2 ..... This bit controls the delay for triggering the "Watchdog". If D2=1, this delay is 1.6 seconds; it is 100 ms if D2 = 0

D3 ..... Initial window address (A15).
D4 ..... Initial window address (A16).
D5 ..... Initial window address (A17).
D6 ..... Initial window address (A18).
D7 ..... Initial window address (A19).
These bits define the address of the 32 Kbyte initial logical memory page as seen by the PC. The other address bits A20, A21, A22 and A23 are forced to 0 during this operation.

Warning: writing to this register for the first time automatically validates the Bus Master mode for PC access towards the MCX-*Lite/*0 card. You must have set channel 0 of DMA controller number 1 to cascade mode before writing to this register.
If you access this register before initializing the Bus Master mode, all PC access to the dual-ported memory will be blocked (as well as the PC!).
You should also note that this logical page is only valid until the host PC sets another page.

* **Address 505h - Restart the "Watchdog" - (Write only):**

D0 set to 0 or 1 ..... Restarts (refreshes) the "Watchdog" timer.

* **Address 506h - Control the "Watchdog" - (Write only):**

D0 set to 0 ..... "watchdog" disabled.
D0 set to 1 ..... "watchdog" enabled.

The "watchdog" may still be disabled by ST1. If the jumper at ST1 is set to position 2-3, the "watchdog" is disabled, whatever the contents of the control register. In position 1-2, however, the "watchdog" may be enabled and disabled according to the contents of the control register.

* **Address 507h - FIFO / PAGE - (Read/Write):**

When reading:

When reading, bits D0 to D7 indicate which 32 Kbyte page has been selected by the PC as dual-ported memory.
Bits D0 to D7 have the following meaning:

D0 ..... Window address (A15)
D1 ..... Window address (A16)
D2 ..... Window address (A17)
D3 ..... Window address (A18)
D4 ..... Window address (A19)
D5 ..... Window address (A20)
D6 ..... Window address (A21)
D7 ..... Window address (A22)

Address bit A23 is always hard-wired to 0 on the MCX-*Lite*/0 card.

1st MEGABYTE				2nd MEGABYTE	
Window address (Hex)	**PAGE register (Hex)**	**Window address (Hex)**	**PAGE register (Hex)**	**Window address (Hex)**	**PAGE register (Hex)**
00000	00	80000	10	100000	20
08000	01	88000	11	108000	21
10000	02	90000	12	110000	22
18000	03	98000	13	118000	23
20000	04	A0000	14	120000	24
28000	05	A8000	15	128000	25
30000	06	B0000	16	130000	26
38000	07	B8000	17	138000	27
40000	08	C0000	18	140000	28
48000	09	C8000	19	148000	29
50000	0A	D0000	1A	150000	2A
58000	0B	D8000	1B	158000	2B
60000	0C	E0000	1C	160000	2C
68000	0D	E8000	1D	168000	2D
70000	0E	F0000	1E	170000	2E
78000	0F	F8000	1F	178000	2F

Excerpt of the correspondence table between window addresses and the Page register.

When writing:

When writing, port 507h lets you write to the FIFO register, which may contain 256 bytes.

III.3.2 Input/Output ports on the host PC

The base input/output (I/O) address of the MCX-*Lite*/0 card for the host PC is set by the DIP switch SW1. The factory setting for the base I/O address is 280h.

* **Address Base + 0 - Read FIFO - (Read only):**

  This I/O port lets you read the contents of the FIFO buffer which was previously filled by the MCX-*Lite*/0 card (this FIFO buffer is 256 bytes deep). If the buffer is empty the value obtained is 0FFH (255).

* **Address Base + 0 - RESET MCX-*Lite*/0 - (Write only):**

  This I/O port lets you "reset" the MCX-*Lite*/0 card. This reset occurs 1.6 seconds after writing to this address. This feature is only available on REV C cards and later, with the Watchdog jumper set (ST1 in position 1-2). Warning: validating the watchdog by software has no effect.

* **Address Base + 1 - Write PAGE - (Write only):**

  Bits D0 to D7 let you select a logical 32 Kbyte page in the memory of the MCX-*Lite*/0 card that will be accessible in the PC window.

  D0 ..... Logical page address- A15.
  D1 ..... Logical page address- A16.
  D2 ..... Logical page address- A17.
  D3 ..... Logical page address- A18.
  D4 ..... Logical page address- A19.
  D5 ..... Logical page address- A20.
  D6 ..... Logical page address- A21.
  D7 ..... Logical page address- A22.

  Address bit A23 is hard-wired to 0 on the MCX-*Lite*/0 card. Warning: writing to this register the first time disables the page selection performed by the MCX-*Lite*/0 card during its initialization.

* **Address Base + 2 - PC TO MCX-*Lite*/0 Int - (Write only):**

  Writing to this address triggers an interrupt to the MCX-*Lite*/0 card (IRQ9 line on the card). This is an alternate method for waking up the MCX-*Lite*/0 card at the interrupt generated when writing to addresses 0 and 1 in the dual-ported memory.
  The contents of the data bits are not significant.

*** Address Base + 3 - Clear MCX-*Lite*/0 TO PC IT:**

When writing:

Writing to this address resets the interrupt generated by the MCX-*Lite*/0 and aimed at the host PC. The contents of the data bits are not significant.

When reading:

Reading this register returns the following information:

D0..... MCX-TO-PC-INT Bit:
when set to 0, this bit indicates that the interrupt signal generated by the MCX-*Lite*/0 card (D Type Flip-Flop address 500H) is idle. When the signal is active this bit equals 1.

D1..... FIFO-EMPTY Bit:
set to 0, it indicates that the FIFO buffer is empty; set to 1, it indicates that the FIFO buffer contains at least one byte.

D2..... MCX-INT Bit:
set to 1, it indicates that the MCX-*Lite*/0 card has not yet disabled the interrupt generated by the PC.

D3..... WIN-SET Bit:
set to 0, this bit indicates that the MCX-*Lite*/0 card has set its initial logical page and that the data read in the PC window is valid. Set to 1, it indicates that this operation has not yet taken place, or that the host PC has selected a new logical page in the window.

D4..... ST2 Bit:
set to 1, it indicates that the ST2 jumper on the MCX-*Lite*/0 card is in position 1-2; set to 0, the jumper is in 2-3.

D5..... ST3 Bit:
set to 1, it indicates that the ST3 jumper on the MCX-*Lite*/0 card is in position 1-2; set to 0, the jumper is in 2-3.

Bits D6 and D7 are not significant.

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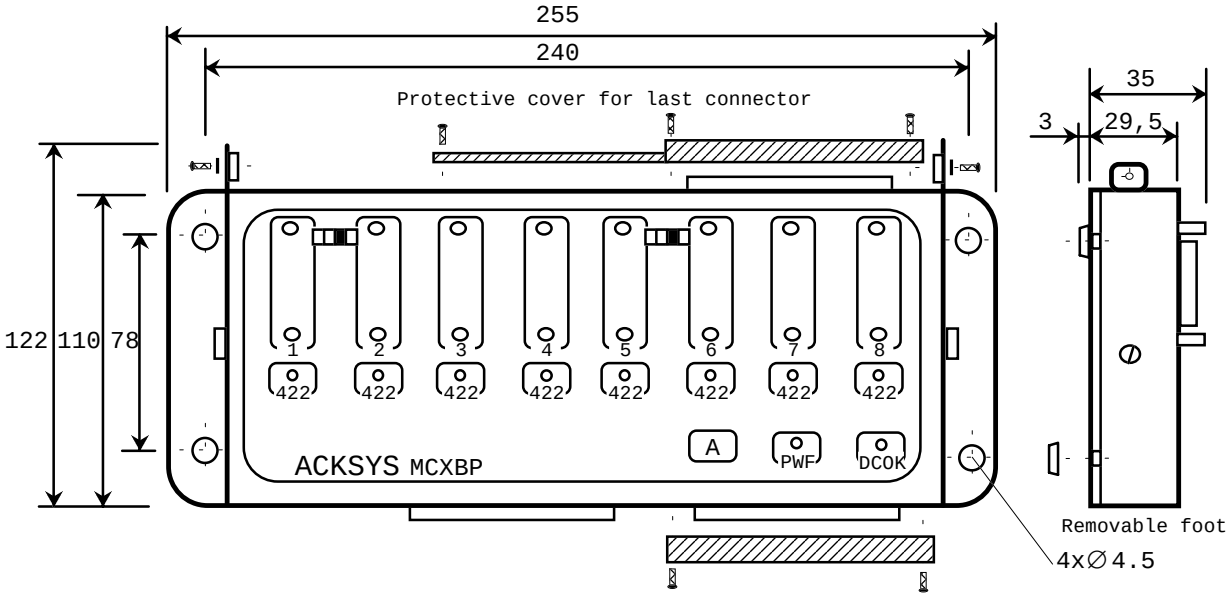
IV. THE MCX-BP EXTENSION



MCX-BP EXTENSION
DIMENSIONS IN mm
WEIGHT = 970 g + 40 g (protective covers for connectors)

The MCX-BP attachment device (RS232D/RS422A) is a fully-independent sub-assembly of the MCX-00 card.

It includes all the communications logic (in particular the ZILOG 85C30 communications processors) as well as the signal amplification system to meet the RS232D and the RS422A standards.

Furthermore, the MCX-BP includes several protective measures for the MCX-BP unit: in particular, resettable fuses provide protection against short circuits, and the Transient Voltage Suppressors (TVS) protect against voltage spikes. They also provide excellent protection against static electricity.

The MCX-BP extension lets you add 8 additional communication lines to the MCX-00 card (up to 8 extensions may be attached to a single MCX-00 card, for a total of 64 channels).

The basic kit includes:

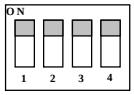
- a device that adds 8 additional lines,
- a kit including screws and protective covers.

IV.1 Configuring the extension

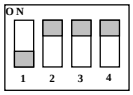
The MCX-BP extension includes two sets of switches[1] located on the rear panel. The first set of four switches lets you select the extension's unit number. The second set, with eight switches, allows to set the lines terminations on the last unit in the chain.

The unit number selected for each extension determines the position of the unit in the daisy chain.

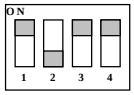
The first MCX-BP unit (lines 1-8) must always be unit number 0.
The figures below illustrate how to configure the 4 switches according to the number of channels attached to the MCX card.



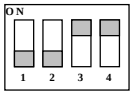
MCX-BP #1 (channels 1 to 8)



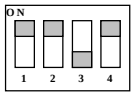
MCX-BP #2 (channels 9 to 16)



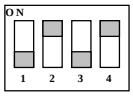
MCX-BP #3 (channels 17 to 24)



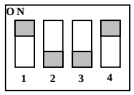
MCX-BP #4 (channels 25 to 32)



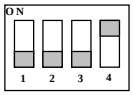
MCX-BP #5 (channels 33 to 40)



MCX-BP #6 (channels 41 to 48)



MCX-BP #7 (channels 49 to 56)



MCX-BP #8 (channels 57 to 64)

All of the eight switches on the last unit in the chain must be set to ON. The eight switches on all the other units must be OFF.
The dot on the two switches located on the front panel should not be visible except for special cases (see section IV.5 " Signals on the Connectors").

[1] When a full configuration is delivered (MCX-00 card + chassis), each chassis is factory-configured.

Checking the configuration of the MCX-BP connection devices

Each eight-channel MCX-BP connection device includes 10 LEDs.

Eight yellow LEDs (one per channel) indicate the configured mode for each of the 8 channels on the MCX card:

- Yellow LED on..... Associated channel configured in RS422A mode.
- Yellow LED off ..... Associated channel configured in RS232D mode.

When the green LED is on, it indicates that the unit is receiving power from the PC or the MCX-PWS power supply.

This light may go out for the following reasons:

- Bad connection in the attachment cable.
- Failure in the +12V or -12V voltages in the system.
- Short circuit on a SUB D 25 pin connector.
- Power supply overload on the SUB D 25 pin connectors.
- LED failure.

In MCC emulation mode only, if the red LED stays on, it indicates that there are more than two MCX-BP units installed, or that more than 8 RS422A lines are active simultaneously; in this case, you must add an external power supply such as the MCX-PWS.

Checking the configuration of the MCX card in MCC emulation mode (jumpers ST2 and ST3 in position 1-2)

If, during the power-on self test, the LEDs display binary code 81h, the configuration of the MCX-BP extensions is incorrect.
If another error code is displayed (see the "Power-on self test" appendix), you must turn off the machine and contact your dealer, who will take all measures necessary to remedy the situation as quickly as possible.

Important note:
If the MCX-00 card is configured in MCXDOS mode (ST2 and ST3 in position 2-3) or in "stand-alone" mode (ST2 in position 2-3 and ST3 in position 1-2), no checks are performed on the configuration of the MCX-BP extensions.

IV.2 Revision history of the extension

- MCX-BP Unit REV D:	A 14.7456 Mhz oscillator was added.
- MCX-BP Unit REV E:	Access to the RING INDICATOR signal in synchronous mode. The RS232 TXCLOCK signal is moved from pin 15 to pin 24. Pin 15 receives an RS-232 incoming transmit clock signal TXCLK_I.

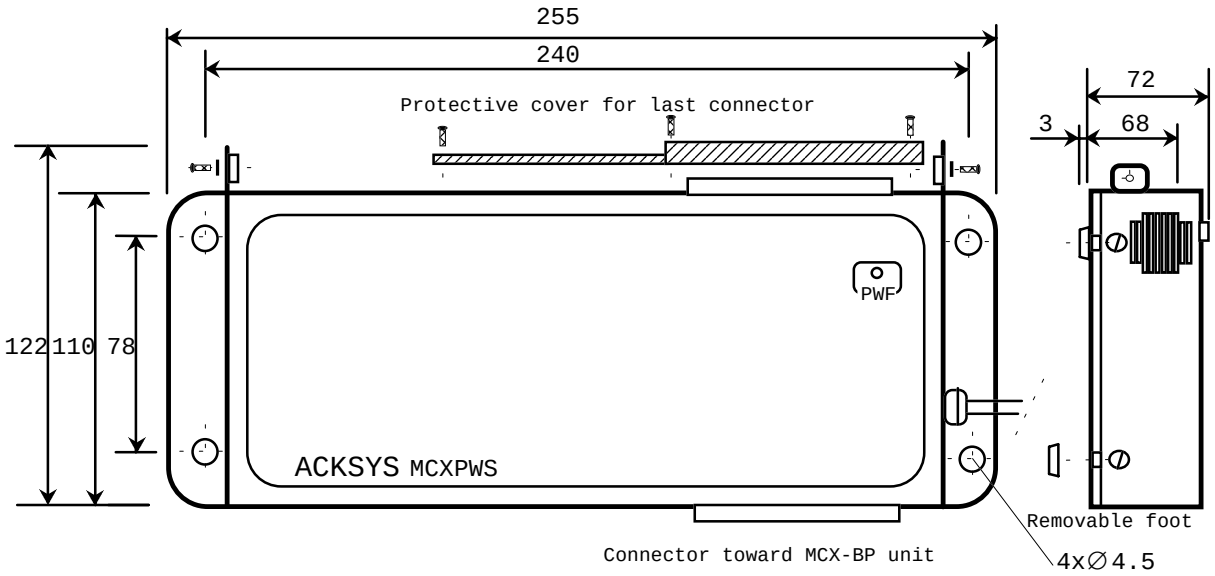
IV.3 Installing the extensions

Once you have installed the card inside the machine, while the power is still off, you must attach the round 80-pin shielded cable between the MCX-00 card and the first MCX-BP connection device.

If you plan to add more than two MCX-BP units, or if you intend to use more than eight RS422A lines simultaneously, you must obtain an MCX-PWS auxiliary external power supply. This will avoid overloading your system's power supply (this external power supply is automatically included in the MCX 24, 32, 40, 48, 56 and 64-channel configurations).

This power supply has the same dimensions as a connection unit. It must be inserted in the middle of the daisy chain of MCX-BP units. This power supply must be plugged in to the mains.

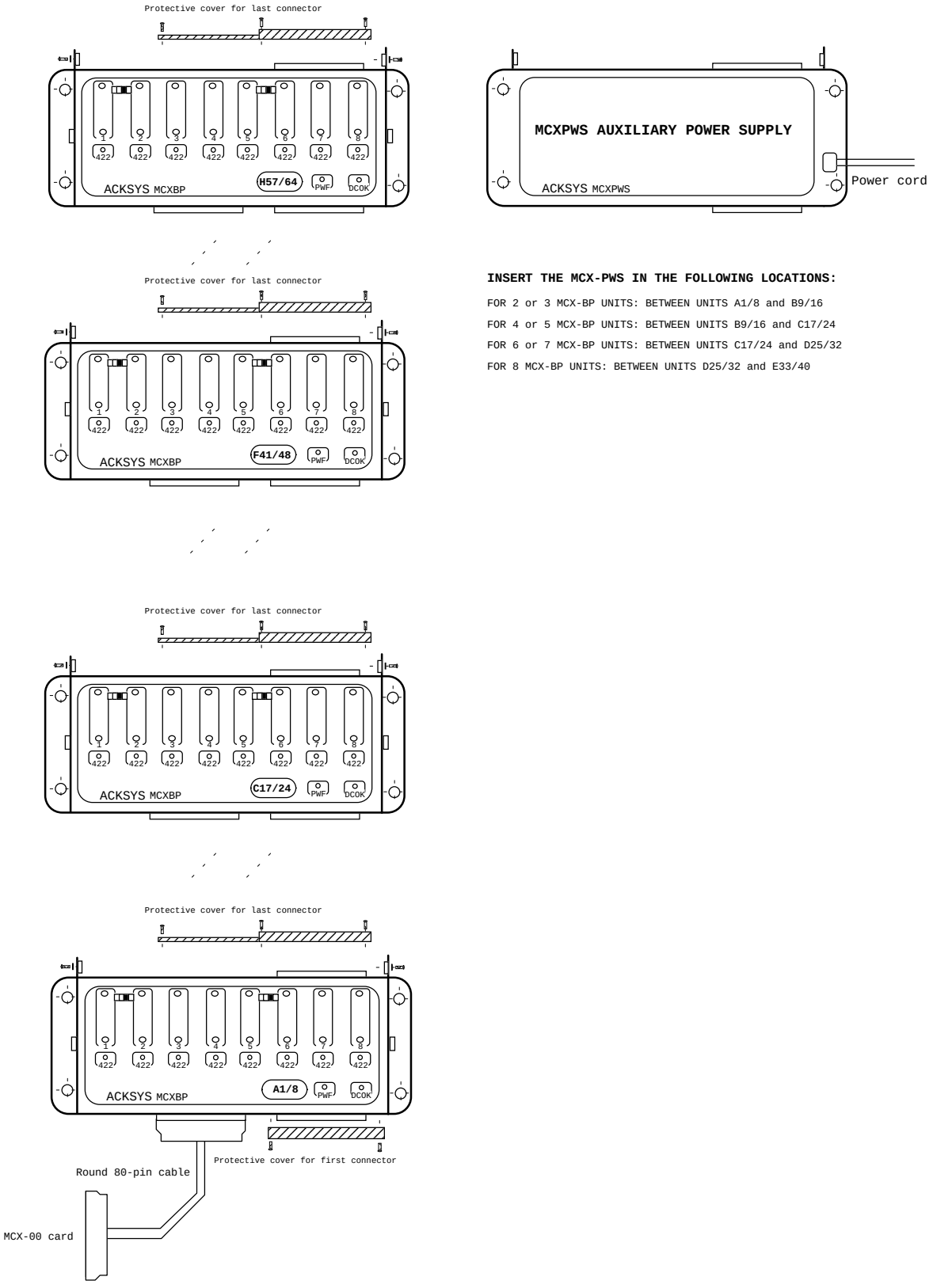
Never connect or disconnect units when your system or the MCX-PWS power supply is powered on.



MCXPWS AUXILIARY POWER SUPPLY
DIMENSIONS IN mm
WEIGHT = 1728 g + 22 g (protective covers for connectors)

CONNECTING FROM 1 TO 8 MCX-BP UNITS

For configurations with more than 16 channels, each MCX-BP unit is identified by a code (A1/8, B9/16, C17/24 ...) printed on a label attached to the front panel, to facilitate the order of assembly.



INSERT THE MCX-PWS IN THE FOLLOWING LOCATIONS:

FOR 2 or 3 MCX-BP UNITS: BETWEEN UNITS A1/8 and B9/16

FOR 4 or 5 MCX-BP UNITS: BETWEEN UNITS B9/16 and C17/24

FOR 6 or 7 MCX-BP UNITS: BETWEEN UNITS C17/24 and D25/32

FOR 8 MCX-BP UNITS: BETWEEN UNITS D25/32 and E33/40

IV.4 Mechanical options

You may reinforce the attachments between the MCX-BP and MCX-PWS units using strengthening rods.

- modulo 2 BP support: to attach 2 units.
- modulo 3 BP support: to attach 3 units.

These supports may be connected together to hold a set of eight MCX-BP units and an MCX-PWS unit.

The MCX-BP and MCX-PWS units may be mounted in a 19" rack with the following supports:

- 19″ Front panel modulo 2 (<5U).
- 19″ Front panel modulo 3 (<8U).
- 19″ Front panel connector (for the round cable) (<3U).

A single MCX-BP unit may be mounted in a 19" rack using the following support:

- MCX-BPRACK (3U).

When operating independently, an MCX card, its power supply and its MCX-BP unit may be mounted in a 19" rack using the following support:

- MCX-RACK 19″ (3U).

IV.5 Signals on the Connectors

SUB D25 PIN CONNECTOR (common to all eight channels of the extension)

Pin #	Signal Direction	Description	CCITT V 24 Standard
1	I	PGND	101
2	O	TXDATA	103
3	I	RXDATA	104
4	O	RTS	105
5	I	CTS	106
6	.	.....	
7	I	GND 0V	102
8	I	CD	109
9	O	+ 12 VDC	
10	O	- 12 VDC	
11[1]	I	+ RXCLOCK	
12	O	- TXDATA	
13	O	+ TXDATA	

Pin #	Signal Direction	Description	CCITT V 24 Standard
14[2]	O	- TXCLOCK	
15[3]	O	TXCLOCK (Rev.<E)	113
	I	TXCLK-I (Rev.≥E)	114
16[1]	O	+ TXCLOCK	
17	I	RXCLOCK	115
18	.	.....	
19[1]	I	- RXCLOCK	
20	O	DTR	108.2
21	I	- RXDATA	
22	I	RI	125
23	I	+ RXDATA	
24	.	..... (Rev <E)	
	O	TXCLOCK (Rev. ≥E)	113
25	.	.....	

I: Input signals
O: Output signals

Warning: to use the ACYSYS AD422/485-INT and BC20MA-INT adapters, you must connect the AUX -12V signal (dot visible on the switch).

The + 12 VDC and - 12 VDC outputs are protected by thermal fuses; the maximum acceptable total intensity for an 8-channel device is 750 mA on each output (which is distributed across the number of loaded channels).

[2] The +RXCLOCK, -RXCLOCK, +TXCLOCK, -TXCLOCK RS422A signals are only available on channels 1 to 3 of each connection device.
The +TXDATA, -TXDATA, +RXDATA and -RXDATA signals are available on all ports if they have been initialized in RS422A mode.

[3] For ports 1 and 5, the two sets of switches located on the front panel of the MCX-BP extension let you select between the following signals for pin 15: TXCLOCK (or TXCLK-I depending on the revision of the MCX-BP) and - 12VDC. The TXCLOCK signal (or TXCLK-I depending on the revision of the MCX-BP) is always active on the other ports.
The -12VDC signal is active when the dot is visible on the switch.

CLOCK SOURCES IN SYNCHRONOUS MODE

For channels programmed in RS232D mode:

3 RS232D clock signals are available on the 25 pin connectors of the MCX-BP unit rev E and later:

- Pin #15 TXCLK_I (Incoming transmit clock signal).
- Pin #17 RXCLK (Incoming receive clock signal).
- Pin #24 TXCLK (Outgoing transmit (and/or) receive clock signal).

2 RS232D clock signals are available on the 25 pin connectors of the MCX-BP unit rev A to rev D:

- Pin #15 TXCLK (Outgoing transmit (and/or) receive clock signal).
- Pin #17 RXCLK (Incoming receive clock signal).

For channels programmed in RS422A mode:

2 RS422A clock signals are available only on the first three 25 pin connectors of the MCX-BP unit:

- Pins #14 and #16 ±TXCLOCK (Outgoing transmit clock signal).
- Pins #19 and #11 ±RXCLOCK (Incoming receive clock signal).

WARNING

The MCX-BP unit has been designed to communicate in either RS232D or RS422A. As a result, the SUB D 25 pin connector uses additional pins compared to standard RS232 connectors.

Consequently, we strongly recommend that you check the assignment of pins 9, 10 and 15 on the connectors of any peripherals you attach to the connection device of the MCX card. Some modems use these pins (in particular pin 9 which is the "Positive Voltage Test") to obtain power for their electronics.

If this is the case, we advise you not to cable this pin, or to check that the modem's power consumption is compatible with the current available (750 mA MAX).

Furthermore, it is absolutely **forbidden** to attach modems or "NULL MODEM" cables to the MCX-BP extension ports without using the adapter cable illustrated below:

MCX-BP rev ≥ E	**MODEM**	**MCX-BP rev < E**	**MODEM**
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
7	7	7	7
8	8	8	8
15	15		
17	17	17	17
20	20	20	20
22	22	22	22
24	24	15	24

This type of cable may be used both for traditional asynchronous modems and BSC or X25 synchronous modems. It cannot damage either piece of equipment (in RS232D only).

IV.6 Electrical and mechanical specifications

Electrical and mechanical specifications for attaching the MCX-BP alone

POWER CONSUMPTION			DIMENSIONS	OPERATING CONDITIONS		
+ 5 V DC	+ 12 V DC	- 12 V DC	Length x Width	Relative humidity (not condensing)	Temperature	Storage
0.8 A max / 4 W	83 mA max / 1 W	83 mA max / 1 W	255mm x 110mm	95% at +25°C	-5 to +65°C	-25 to +70°C

Electrical and mechanical specifications for the MCX-00 card with from 1 to 8 MCX-BP units

TOTAL POWER CONSUMPTION (MCX-00 + 1 to 8 MCX-BP units)	
+ 5 V for 8 lines	2.4 A max /12 W
+ 5 V for 16 lines	3.2 A max /16 W
+ 5 V for 24 lines[1]	1.6 A max /8 W
+ 5 V for 32 lines[1]	1.6 A max /8 W
+ 5 V for 40 lines[1]	1.6 A max /8 W
+ 5 V for 48 lines[1]	1.6 A max /8 W
+ 5 V for 64 lines[1]	1.6 A max /8 W
+ 12 V for 8 lines	83 mA max / 1 W
+ 12 V for 16 lines	166 mA max / 2 W
+ 12 V for 24 lines[1]	0 mA max / 0.00 W
+ 12 V for 32 lines[1]	0 mA max / 0.00 W
+ 12 V for 40 lines[1]	0 mA max / 0.00 W
+ 12 V for 48 lines[1]	0 mA max / 0.00 W
+ 12 V for 64 lines[1]	0 mA max / 0.00 W
- 12 V for 8 lines	83 mA max / 1 W
- 12 V for 16 lines	166 mA max / 2 W
- 12 V for 24 lines[1]	0 mA max / 0.00 W
- 12 V for 32 lines[1]	0 mA max / 0.00 W
- 12 V for 40 lines[1]	0 mA max / 0.00 W
- 12 V for 48 lines[1]	0 mA max / 0.00 W
- 12 V for 64 lines[1]	0 mA max / 0.00 W

Power consumption calculations are based on an MCX-00 card with an 80386 SX 25 Mhz processor, an 80387 25 Mhz coprocessor, 4 Mbytes RAM and from 1 to 8 MCX-BP units with 8 RS422A channels with no load.

[1] Power consumption is lower for configurations with more than 16 channels, since the MCX-PWS auxiliary power supply is used systematically.
This auxiliary power supply is required for more than 16 channels, or when there are more than 8 RS422A lines active simultaneously.
When the MCX-PWS external power supply is connected, total power consumption on the PC bus is equivalent to the power consumed by the MCX card plus whatever the number of lines installed.

IV.7 Programming

This information is provided only for writing programs that are internal to the card.

IV.7.1 Input/Output ports on the MCX-BP unit

Up to 8 RS232D / RS422A connection units may be attached to one MCX card. Each unit has its own address range and interrupt level:

- Unit #1: Addresses 600h to 61Fh, IRQ3.
- Unit #2: Addresses 620h to 63Fh, IRQ4.
- Unit #3: Addresses 640h to 65Fh, IRQ5.
- Unit #4: Addresses 660h to 67Fh, IRQ6.
- Unit #5: Addresses 680h to 69Fh, IRQ7.
- Unit #6: Addresses 6A0h to 6BFh, IRQ11.
- Unit #7: Addresses 6C0h to 6DFh, IRQ12.
- Unit #8: Addresses 6E0h to 6FFh, IRQ14.

In each unit the addresses are distributed as follows:

* SCC # 0
  - Base address + 00h Channel 2, command register - (Read/write).
  - Base address + 01h Channel 2, data register - (Read/write).
  - Base address + 02h Channel 1, command register - (Read/write).
  - Base address + 03h Channel 1, data register - (Read/write).

* SCC # 1
  - Base address + 04h Channel 4, command register - (Read/write).
  - Base address + 05h Channel 4, data register - (Read/write).
  - Base address + 06h Channel 3, command register - (Read/write).
  - Base address + 07h Channel 3, data register - (Read/write).

* SCC # 2
  - Base address + 08h Channel 6, command register - (Read/write).
  - Base address + 09h Channel 6, data register - (Read/write).
  - Base address + 0Ah Channel 5, command register - (Read/write).
  - Base address + 0Bh Channel 5, data register - (Read/write).

* SCC # 3
  - Base address + 0Ch Channel 8, command register - (Read/write).
  - Base address + 0Dh Channel 8, data register - (Read/write).
  - Base address + 0Eh Channel 7, command register - (Read/write).
  - Base address + 0Fh Channel 7, data register - (Read/write).

* **Base address + 10h - Polling Register (read only):**

The polling register identifies SCCs whose interrupt line is active.

D0 to 1 ..... SCC # 0 is active.
D1 to 1 ..... SCC # 1 is active.
D2 to 1 ..... SCC # 2 is active.
D3 to 1 ..... SCC # 3 is active.

D4 ..... PWEXT Bit: if set to 0, this bit indicates that an external MCX-PWS power supply is attached to the daisy chain of units.
In the opposite case, this bit is set to 1 to indicate that there is no power supply or that the power supply unit is turned off.

D6 ..... Status of the clock source (BP rev D and later +):
- 1: SCC clock = 16 Mhz,
- 0: SCC clock = 14.7456 Mhz.

D7 ..... Terminal Count (DMA)
If this bit is set to 1, it indicates that a DMA cycle has just completed for a line of this unit. This bit is automatically reset to 0 if you read the address of the polling register + 1 (Base + 11h).
Warning: this register cannot be used to identify the DMA channel that just finished its cycle when several cycles finish at the same time; in that case, read the status registers of the various DMA controllers.
Finally, the "Terminal count" automatically generates an interrupt to the MCX card on the same line as the SCCs.

These bits are all set to zero after an SCC RESET.

* **Base address + 11h - Reset T/C bit (Read only):**

Reading this address zeroes the T/C bit that is read-latched to the polling register.

* **Base address + 12h - Read RING (Read only):**

This register only exists in versions E and later of the MCX-BP unit. It lets you read the RING INDICATOR signal when the lines in question are operating in synchronous mode.
Each bit in this register set to 1 indicates that the RING signal is active on the line associated to this bit (Bit 0 = Line 1, Bit 1 = Line 2, etc.).

* **Base address + 14h - RS232D/RS422A Configuration (Write only):**

The 8 bits in this register let you configure each of the unit's eight connection channels in RS232D or RS422A mode.

D0 ..... Channel 1.
D1 ..... Channel 2.
D2 ..... Channel 3.
D3 ..... Channel 4.
D4 ..... Channel 5.
D5 ..... Channel 6.
D6 ..... Channel 7.
D7 ..... Channel 8.

Each bit set to 1 forces the channel concerned to operate in RS422A mode rather than in RS232D mode.

* **Base address + 15h - DMA / Clock Configuration (Write only):**

The first three bits of this register (D0, D1 and D2) let you assign the MCX card's DMA channels to lines 1, 2 and 3 as follows:

D0 to 1 ..... Channel 1 with DRQ1 and DRQ2.

D1 to 1 ..... Channel 2 with DRQ3 and DRQ5.

D2 to 1 ..... Channel 3 with DRQ6 and DRQ7.
When these bits are set to 0, the associated DMA channels are virtually disconnected from the communication lines. This lets you, for example, use line 1 in DMA mode for the first unit, but use lines 2 and 3 in DMA mode for the second unit.

In any case, the first DMA channel must be used to transmit while the second may only be used to receive.

Warning: DMA channels DRQ1, DRQ2 and DRQ3 are 8-bit channels while channels DRQ5, DRQ6 and DRQ7 are 16 bit-channels.

D3 ..... Power Fail LED Command.
When this bit is set to 1, the Power Fail LED on the connection unit is turned on.

D7 ..... SCC source clock command:
- 0 for 16 Mhz,
- 1 for 14.7456 Mhz.
Only on MCX-BP revision D cards and later

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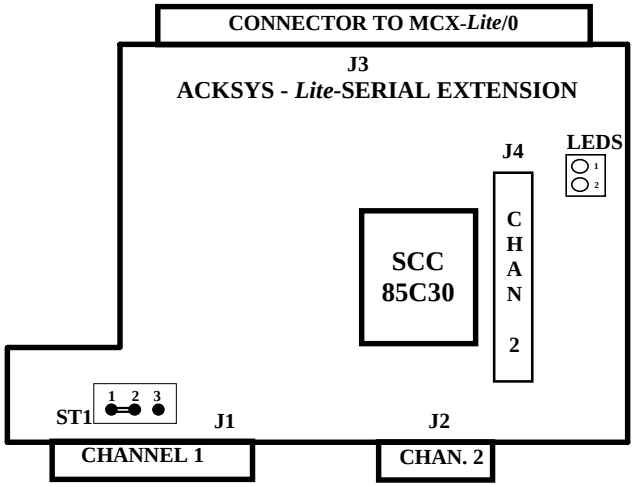
V. THE *LITE*-SERIAL EXTENSION

If you add the *Lite*-SERIAL extension to the MCX-*Lite*/0 card, the result is equivalent to the MCX-*Lite*/S card.

The *Lite*-SERIAL extension includes all the communications logic (in particular a ZILOG 85C30 communications processor) as well as line drivers required by the RS232D and RS422A standards.

This extension lets you add two asynchronous or synchronous RS232D or RS422A channels to the MCX-*Lite*/0 card, which then performs like one-quarter of an MCX-08 card.



Factory settings ..... ST1 in position 1-2

V.1 Configuring the extension

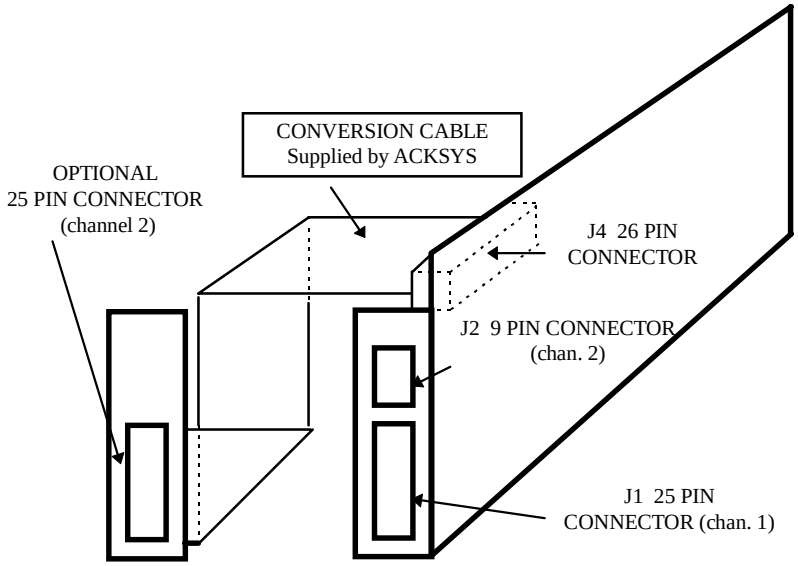
- **ST1**
  The ST1 jumper either enables or disables the presence of the +12 power supply on the J1 and J4 output connectors.

  In position 1-2 this voltage is not available; in position 2-3 +12V is available on connectors J1 and J4 as described below:

  - J1 ..... Pin 9,
  - J4 ..... Pin 17.

V.2 Installing the MCX-*Lite*/S card in the PC

Leave a free slot near the card in case you wish to replace the J2 SUB D9 connector with a SUB D25 pin connector.



If the SUBD 9 pin connector is replaced by a SUBD 25 pin connector, both of the card's channels have the same connections.

V.3 Signals on the Connectors

The MCX-*Lite*/S card offers 3 output connectors:

- **J1 connector and the optional SUBD 25 pin connector**
  These 25 pin male connectors are connected to lines 1 and 2 on the card.

J1 SUB D25 PIN CONNECTOR - LINE 1 - and OPTIONAL SUB D25 PIN CONNECTOR - LINE 2

Pin #	Signal Direction	Description	CCITT V 24 Standard
1	I	PGND	101
2	0	TXDATA	103
3	I	RXDATA	104
4	0	RTS	105
5	I	CTS	106
6	.	.....	
7	I	GND 0V	102
8	I	CD	109
9[1]	0	+ 12 VDC (250 mA)	
10	0	.....	
11	I	+RXCLOCK	
12	0	-TXDATA	
13	0	+TXDATA	

Pin #	Signal Direction	Description	CCITT V 24 Standard
14	0	-TXCLOCK	
15	I	TXCLK-I	114
16	0	+TXCLOCK	
17	I	RXCLOCK	115
18	.	.....	
19	I	-RXCLOCK	
20	0	DTR	108.2
21	I	-RXDATA	
22	I	RI	125
23	I	+RXDATA	
24	O	TXCLOCK	113
25	.	.....	

I: Input signal - O: Output signal

- **J2 Connector**
  This SUBD 9 pin male connector is attached to the second line.

J2 SUB D9 PIN CONNECTOR - LINE 2

Pin #	Signal Direction	Description
1	I	CD
2	I	RXDATA
3	O	TXDATA
4	O	DTR
5	I	GND 0V
6	.	.....
7	O	RTS
8	I	CTS
9	I	RI

I: Input signal - O: Output signal

[1]Power available if the ST1 jumper on the *Lite*-SERIAL extension is in position 2-3.

- **J4 Connector**
  The J4 connector is provided (HE 10 26 pins) because it is not possible to output all the RS232D and RS422A signals on the J2 connector. You may directly attach a ribbon cable equipped with a standard SUB D25 pin connector to J4.

J4 HE 10 26 PIN CONNECTOR - LINE 2

Pin #	Signal Direction	Description	CCITT V 24 Standard	Pin #	Signal Direction	Description	CCITT V 24 Standard
1	I	PGND	101	14	O	DTR	108.2
2	O	-TXCLK		15	I	CD	109
3	O	TXDATA	103	16	I	-RXDATA	
4	I	TXCLK-I	114	17[1]	O	+ 12 VDC	
5	I	RXDATA	104	18	I	RI	125
6	O	+TXCLK		19	.	.....	
7	O	RTS	105	20	I	+RXDATA	
8	I	RXCLK	115	21	I	+RXCLK	
9	I	CTS	106	22	O	TXCLK	113
10	.	.....		23	O	-TXDATA	
11	.	.....		24	.	.....	
12	I	-RXCLK		25	O	+TXDATA	
13	I	GROUND 0V	102	26	.	.....	

I: Input signal - O: Output signal

CLOCK SOURCE IN SYNCHRONOUS MODE

If channel 2 is operated in synchronous mode, it is indispensable to use the optional SUBD 25 pin connector.

For channels programmed in RS232D mode:
3 RS232D clock signals are available on the 25 pin connectors of the *Lite*-SERIAL extension.

- Pin#15 TXCLK_I (Incoming transmit clock signal)
- Pin#17 RXCLK (Incoming receive clock signal).
- Pin#24 TXCLK (Outgoing transmit and/or receive clock signal)

For channels programmed in RS422A mode:
2 RS422A clock signals are available on the 25 pin connectors of the *Lite*-SERIAL extension.

- Pins #14 and #16 ±TXCLOCK (Incoming transmit clock signal).
- Pins #19 and #11 ±RXCLOCK (Incoming receive clock signal).

[1] Power available if the ST1 jumper on the *Lite*-SERIAL extension is in position 2-3.

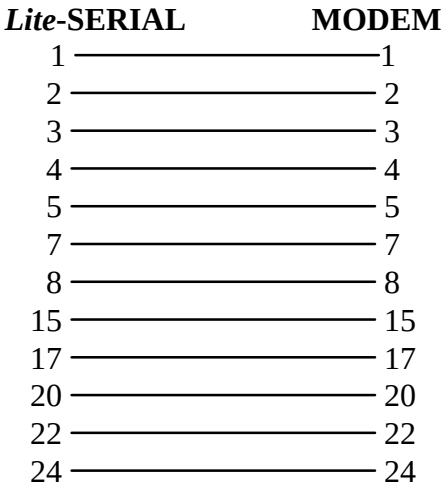
WARNING

The *Lite*-SERIAL extension has been designed to communicate in either RS232D or RS422A. As a result, the SUB D 25 pin connector uses additional pins compared to standard RS232 connectors.

Consequently, we strongly recommend that you check the pin assignments on the connectors of any peripherals you attach to the *Lite*-SERIAL extension. Some modems use these pins (in particular pin 9 which is the "Positive Voltage Test") to obtain power for their electronics.

If this is the case, we advise you not to cable this pin, or to check that the modem's power consumption is compatible with the available current (250 mA MAX).

Furthermore, it is absolutely **forbidden** to attach modems or "NULL MODEM" cables to the *Lite*-SERIAL extension ports without using the adapter cable illustrated below:



This type of cable may be used both for traditional asynchronous modems and BSC or X25 synchronous modems. It cannot damage either piece of equipment (in RS232D only).

V.4 Mechanical options

- MCX-*Lite* 19'' Rack (2U):
  includes an MCX-*Lite*/S card, two SUBD25 connectors and a power supply.

V.5 Electrical and mechanical specifications

Electrical specifications of the Lite-SERIAL extension

POWER CONSUMPTION	
+ 5 V DC	±12 V DC
0.27 A max /1.35 W	18 mA max /216 mW

Electrical and mechanical specifications of the MCX-Lite/S card

POWER CONSUMPTION			DIMENSIONS	OPERATING CONDITIONS		
+ 5 V DC	+ 12 V DC	- 12 V DC	Length x Width	Relative humidity (non-condensing)	Temperature	Storage
1.75 A max / 8.75 W	18 mA max / 216 mW	18 mA max / 216 mW	340mm x 115mm	95% at +25°C	-5 at +65°C	-25 at +70°C

The dimensions do not include the attachment bar and the two ISA connectors.

Power consumption calculations are based on an MCX-*Lite*/S card with an 80386 SX 25 Mhz processor, an 80387 25 Mhz coprocessor, 4 Mbytes RAM and the two serial channels programmed in RS422A mode with no load.

V.6 Programming

This information is provided only for writing programs that are internal to the card.

V.6.1 Input/Output ports on the *Lite*-SERIAL extension

The *Lite*-SERIAL extension card is fully compatible with channels 1 and 2 of an MCX-08. The base address of these channels is set at 600h and cannot be changed. The input/output addresses are as follows:

SCC #0

Address 600h	Channel 2, command register - (Read/write)
Address 601h	Channel 2, data register - (Read/write)
Address 602h	Channel 1, command register - (Read/write)
Address 603h	Channel 1, data register - (Read/write)

* **Address 610h - Polling register (Read only):**

D0..... This bit provides the status of the SCC's interrupt line. It is set to 1 if the SCC interrupt line is active.
Bit D0 is set to zero after an SCC RESET.

D1..... Not significant.

D2..... Not significant.

D3..... Not significant.

D6..... Status of the clock source:
- 1: SCC clock = 16 Mhz,
- 0: SCC clock = 14.7456 Mhz.

D7..... T/C Bit: Terminal Count (DMA)
If this bit is set to 1, it indicates that a DMA cycle has just completed for one of the unit's lines.
This bit is automatically reset to 0 if you read the address of the polling register + 1 (address 611h).
Warning: this register cannot be used to identify the DMA channel that just finished its cycle when several cycles finish at the same time; in that case, read the status registers of the various DMA controllers.
Finally, the "Terminal count" automatically generates an interrupt to the MCX-*Lite*/0 card on the same line as the SCCs.

* **Address 611h - Reset T/C bit (Read only):**

Reading this address zeroes the T/C bit that is read-latched to the polling register.

* **Base address + 12h - Read RING (Read only):**

This register lets you read the RING INDICATOR (RI) signal when the lines in question are operating in synchronous mode.

D0 ..... equals 1 if the RING signal is active on channel 1, 0 if not active.
D1 ..... equals 1 if the RING signal is active on channel 2, 0 if not active.

* **Address 614h - RS232D/RS422A Configuration (Write only):**

The 2 least significant bits in this register let you configure each of the *Lite*-SERIAL extension's two channels in RS232D or RS422A mode.

D0 ..... equals 1 if channel 1 is in RS422A; 0 if the channel is in RS232D.
D1 ..... equals 1 if channel 2 is in RS422A; 0 if the channel is in RS232D.

* **Address 615h - Clock source (Write only):**

This register controls the source of the SCC clock as described below:

D7 ..... SCC clock source command:
- 0 = 16 Mhz,
- 1 = 14.7456 Mhz.

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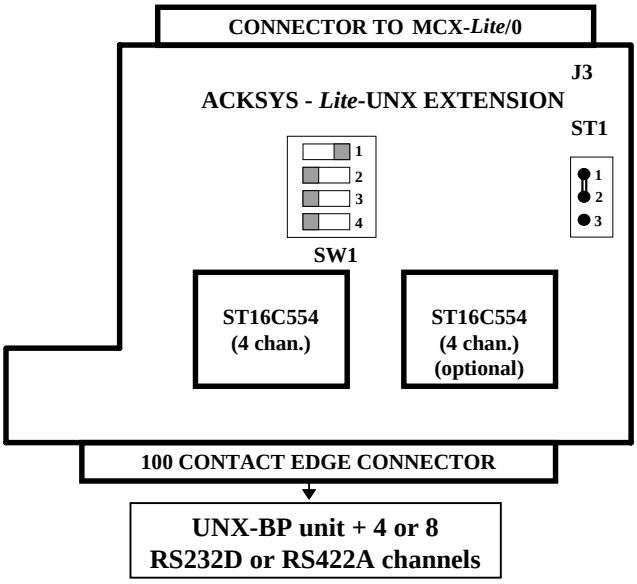
VI. THE *LITE*-UNX EXTENSION

If you add the *Lite*-UNX extension to the MCX-*Lite*/0 card, the result is equivalent to the MCX-*Lite*/U card.

The *Lite*-UNX extension is based on one or two quadruple asynchronous communication units (each unit includes 4 16C550 components) with FIFO buffers that are compatible with the 16450 (8250) used in all PCs.

Quadruple RS422A, RS485 and 20 mA current loop interfaces are also available for industrial environments. The characteristics of the integrated RS422A interface as well as the quadruple RS422A and RS485 interfaces are provided in the Appendix entitled "RS422A-RS485 INTERFACE".

The MCX-*Lite*/U card is equivalent to a PC equipped with an ACKSYS UNX232 card.



Factory settings ..... SW1 = IRQ3 ST1 = 1-2 - Interrupt controlled by the mask register

VI.1 Configuring the extension

The *Lite*-UNX extension includes a set of four switches (SW1) and a three-post jumper (ST1).

SW1 Switch- Interrupts

This set of four switches can be used to configure the interrupt line (with the MCX-*Lite*/0 card) used by the extension. The interrupt selected is common to all channels. You may select one of four interrupt levels (IRQ3, IRQ4, IRQ5 or IRQ7) as described below:

sw1-1	sw1-2	sw1-3	sw1-4
IRQ 3	IRQ 4	IRQ 5	IRQ 7

DIP Switch SW1 - Selecting the interrupt line

An interrupt is selected when the corresponding switch is in the "ON" position.

At the first level, interrupts are controlled for each communications device when bits are set in the 16C550's interrupt register.

- **ST1 Jumper - Mask register**

  Interrupts may also be controlled using the MASK and POLLING registers on the card. These registers are described in the "Programming" section.

  The ST1 jumper validates the use of the mask register.

  ST1 in position 1-2: Mask register enabled.
  ST1 in position 2-3: Mask register disabled.

VI.2 Installing the UNXBP+ unit

The *Lite*-UNX extension is connected to the SUB D 25 pin connectors on the UNXBP+ unit using a round 50-pin shielded cable (4 channel version) or 100-pin cable (8 channel version).

You should check the cable connection. The unit contains active components, and an improper connection is likely to damage the device.

Several types of UNXBP+ extensions are available:

- The 4 channel RS232D extension (channel 1 may be switched to RS422A).
- The 4 channel RS422A extension (channel 1 may be switched to RS232D).
- The 8 channel RS232D extension (channels 1 and 5 are switchable to RS422A).
- The 8 channel RS422A extension (channels 1 and 5 are switchable to RS232D).
- The 8 channel mixed extension, with 4 RS232D channels (channel 1 is switchable to RS422A) and 4 RS422A channels (channel 1 is switchable to RS232D).

When delivered, all the channels in an RS232D unit are configured as RS232D, and all the channels in an RS422A unit are configured as RS422A.

You can configure channels 1 and 5 as follows:
- On the back of the UNXBP+ unit, find the 2 or 3 switches located under the connectors for the channels that are switchable between RS232D and RS422A.
  - If the dots are visible: mode 422 is selected.
  - If the dots are not visible: mode 232 is selected.

These switches are accessible through a slot in the unit cover. **Do not open the unit!** That would void your warranty.

VI.3 Signals on the UNXBP+ Connectors

The following table describes the signals on the 25 pin connector of the UNXBP+ 232 and UNXBP+ 422 units.

Pin #	Signal Direction	Description	CCITT V 24 Standard
1	I	PGND	101
2	O	TXDATA	103
3	I	RXDATA	104
4	O	RTS	105
5	I	CTS	106
6	I	DSR	107
7	I	GND 0V	102
8	I	CD	109
9	O	+POL/ + 12 VDC	
10	O	-POL/ - 12 VDC	
11	.	.....	
12	O	- TXDATA	
13	O	+ TXDATA	

Pin #	Signal Direction	Description	CCITT V 24 Standard
14	.	.....	
15	.	.....	
16	.	.....	
17	.	.....	
18	.	.....	
19	.	.....	
20	O	DTR	108.2
21	I	- RXDATA	
22	I	RI	125
23	I	+ RXDATA	
24	.	.....	
25	.	.....	

I: Input signal - O: Output signal

The +12 VDC and -12 VDC outputs are protected by thermal fuses. The maximum acceptable total load for an 8-channel unit is 750 mA at each voltage level (to be distributed across the number of active channels).

⇒ **Note for UNXBP+ 232 units:**

Warning: the ±TXDATA and ±RXDATA RS422A signals are only available on port 1 of a 4 channel UNXBP+ RS232D extension and on ports 1 and 5 of an 8 channel UNXBP+ RS232D extension, if they have been configured in RS422A. The ±POL signals are not available: they provide ±12V in all modes.

⇒ **Note for UNXBP+ 422 units:**

Warning: the RS232D signals are only available on port 1 of a 4 channel UNXBP+ RS422A extension and on ports 1 and 5 of an 8 channel UNXBP+ RS422A extension, if they have been configured in RS232D mode. The +POL signal is replaced by +12V for channels 1 and 5 programmed in RS232D.

WARNING

We strongly recommend that you check the assignment of pins 9 and 10 on the connectors of any peripherals you attach to the *Lite*-UNX extension connectors. Some modems use these pins to power their electronics.

If this is the case, we advise you not to cable this pin, or to check that the modem's power consumption is compatible with the available current (750 mA MAX).

If a LED is lighted, it indicates that the connectors are correctly powered by the system.

This LED may go out for the following reasons:

- Bad connection in the attachment cable.
- Failure in the +12V or -12V voltages in the system.
- Short circuit on a SUB D 25 pin connector.
- Power supply overload on the SUB D 25 pin connectors.

In case of an accidental short circuit on the SUB D25 pin connectors, you should power down the system and determine the cause of the short circuit.

Warning: you must wait 20 seconds before restoring power to the connection device after shutting down the system. This is due to the resettable protective thermal fuses.

VI.4 Mechanical options

- MCX-*Lite*/UNX 19'' Rack (2U):
  includes an MCX-*Lite*/UNX card, a power supply and four connectors on the front (3 SUBD25 and 1 SUBD9).

VI.5 Electrical and mechanical specifications

Electrical specifications of the *Lite*-UNX extension with UNXBP+ 4 RS232D channels

POWER CONSUMPTION	
+ 5 V DC	±12 V DC
0.2 A max / 1 W	48 mA max / 576 mW

Electrical specifications of the *Lite*-UNX extension with UNXBP+ 8 RS232D channels

POWER CONSUMPTION	
+ 5 V DC	±12 V DC
0.22 A max / 1.1 W	96 mA max / 1.1 W

Electrical and mechanical specifications of the MCX-*Lite*/U card with 4 and 8 RS232D channels

POWER CONSUMPTION			DIMENSIONS	OPERATING CONDITIONS		
+ 5 V DC	+ 12 V DC	- 12 V DC	Length x Width	Relative humidity (non-condensing)	Temperature	Storage
1.68 A max / 8.4 W (4 chan.)	48 mA max / 576 mW (4 chan.)	48 mA max / 576 mW (4 chan.)	340mm x115 mm	95% at +25°C	-5 to +65°C	-25 to +70°C
1.7 A max / 8.5 W (8 chan.)	96 mA max / 1.1 W (8 chan.)	96 mA max / 1.1 W (8 chan.)				

- Maximum output voltage in shared mode (RS422A): ±7V.
- Maximum input voltage in shared mode(RS422A): ±10V.
- Maximum input voltage in differential mode(RS422A): ±12V.
- A 121 Ohm terminating resistor is connected between the +RX and -RX signals.
- Recommended cable: 24 gauge AWG twisted pair + external shielding/braid (BELDEN 8102).

The dimensions do not include the attachment bar and the two ISA connectors.

Power consumption calculations are based on an MCX-*Lite*/U card with an 80386 SX 25 Mhz processor, 4 Mbytes RAM and 4 or 8 serial channels programmed in RS232A mode with no load.

VI.6 Programming

This information is provided only for writing programs that are internal to the card.

VI.6.1 Input/Output ports on the *Lite*-UNX extension

The base address of the *Lite*-UNX extension is set to **280h** and cannot be changed (without changing the PAL decoder). It uses a block of 64 sequential I/O addresses for 8 ports, and 32 addresses for 4 ports.

The base addresses for the various channels are listed below:

PORT 1	PORT 2	PORT 3	PORT 4	PORT 5	PORT 6	PORT 7	PORT 8
280h	288h	290h	298h	2A0h	2A8h	2B0h	2B8h

The characteristics of the 16C550 are described in the appendix.
Two special registers have been added to the *Lite*-UNX extension: the "MASK" and the "POLLING" registers.

- The "POLLING" register contains 8 bits; each bit corresponds to a port. Bits set to 1 indicate that an interrupt has been detected on the corresponding port.

- The "MASK" register is an 8-bit register that lets you disable a single interrupt or a combination of interrupts for each port, without changing the interrupt register on the 16C450.
  To mask (disable) a line's interrupt, write a 0 bit corresponding to the line to disable. To unmask (enable) a line, write a 1 bit.
  To determine which ports triggered the interrupts, you may query the 16C550's interrupt identification registers or the "POLLING" register.

You can access the "MASK" and "POLLING" registers at address 287h.

WRITE MASK REGISTER AT ADDRESS 287h

Bit 0 - Port 1	= 0	Masked	= 1	Unmasked
Bit 1 - Port 2	= 0	Masked	= 1	Unmasked
Bit 2 - Port 3	= 0	Masked	= 1	Unmasked
Bit 3 - Port 4	= 0	Masked	= 1	Unmasked
Bit 4 - Port 5[1]	= 0	Masked	= 1	Unmasked
Bit 5 - Port 6[1]	= 0	Masked	= 1	Unmasked
Bit 6 - Port 7[1]	= 0	Masked	= 1	Unmasked
Bit 7 - Port 8[1]	= 0	Masked	= 1	Unmasked

NOTE:
If jumper ST1 is in position 1-2, all interrupts coming from the *Lite*-UNX extension will be subject to the contents of the mask register; if not, the mask register is ignored.

[1] Significant for an 8 channel card.

READ POLLING REGISTER AT ADDRESS 287h

Bit 0 - Port 1	Interrupt if 1
Bit 1 - Port 2	Interrupt if 1
Bit 2 - Port 3	Interrupt if 1
Bit 3 - Port 4	Interrupt if 1
Bit 4 - Port 5[1]	Interrupt if 1
Bit 5 - Port 6[1]	Interrupt if 1
Bit 6 - Port 7[1]	Interrupt if 1
Bit 7 - Port 8[1]	Interrupt if 1

VI.6.2 Enabling interrupts

You may control interrupts at five levels:

* via the channel interrupt register, evaluated for all interrupt types.
* via the extension's polling register.
* globally for a channel, via the OUT2 bit in its MODEM control register.
* via the 8259 controller on the MCX-*Lite*/0 card, by managing the selected interrupt line.
* using the processor's CLI/STI instructions.

Warning: the 8259 also uses IRQ7 to indicate a "SPURIOUS INTERRUPT" condition.

VI.6.3 Baud rate generator

All the baud rate generators use a common 1.8432 Mhz clock. The transmit and receive clocks are interconnected.

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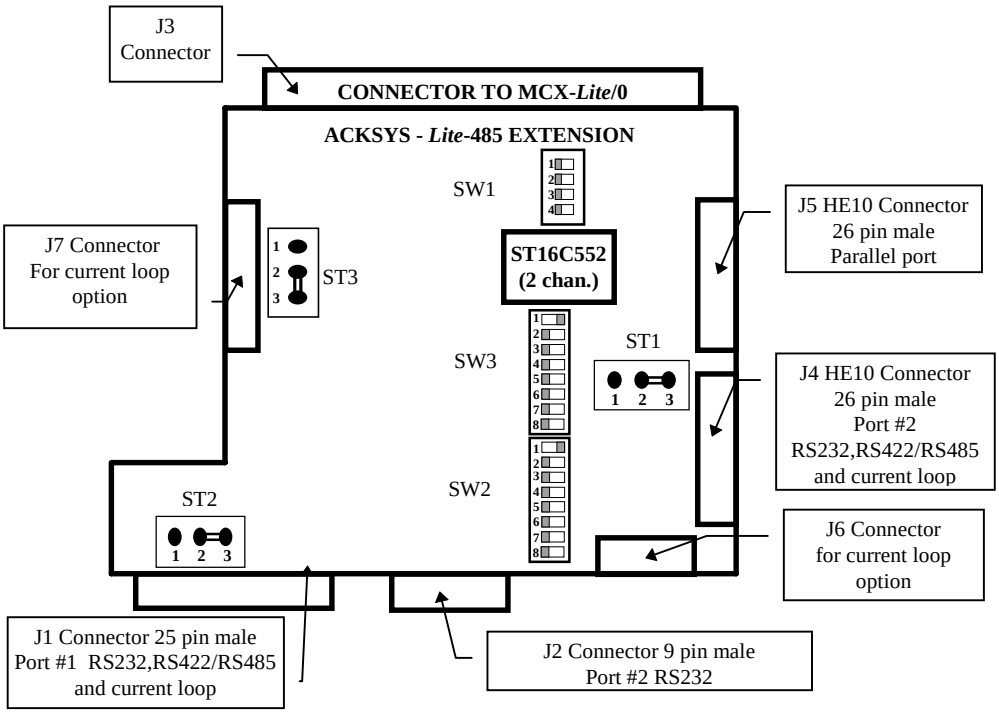
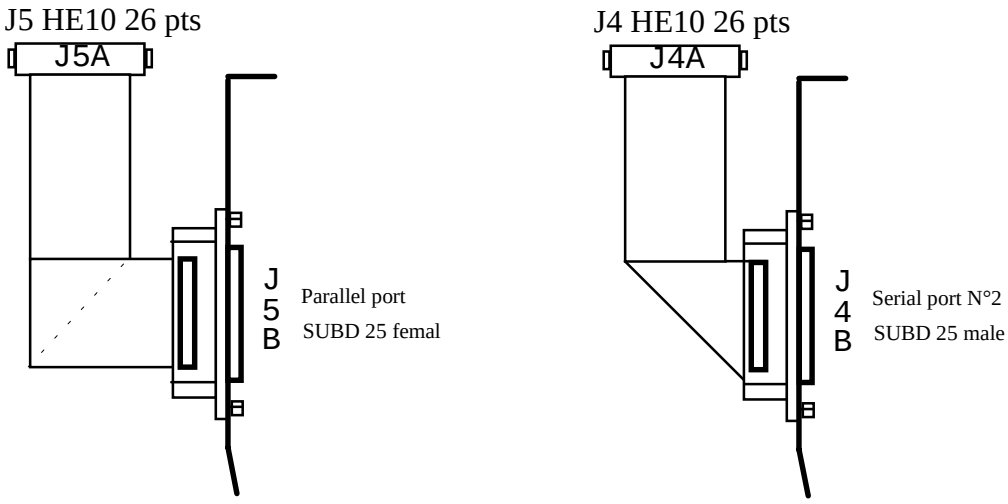
VII. THE *LITE*-485 EXTENSION

If you add the *Lite*-485 extension to the MCX-*Lite*/0 card, the result is equivalent to the MCX-*Lite*/485 card. This card features 2 asynchronous serial ports (up to 115,200 bits/second) for controlling industrial communications lines in RS232, RS422 or RS485.
The *Lite*-485 is based on dual asynchronous communication units (each unit includes 2 16C550 components) with FIFO buffers that are compatible with the 8250 used in all PCs.

The RS232D, RS422A, RS485 and 20 mA current loop interfaces[1] are each available on the 2 extension ports to meet the requirements of industrial environments.
The *Lite*-485 extension also includes a parallel port for connecting a printer or a software protection dongle.





[1] The current loop interface is optional.

Factory settings: Serial port #1 and #2:
- in RS485 mode with ECHO OFF,
- RTS transmission control enabled,
- line polarization,
- terminating resistor,
- interrupts and addresses COM1/COM2 (3F8h,IRQ4/2F8h,IRQ3).

- ST1 = 1-2 - Parallel port configuration: Latched mode,
- ST2 = 1-2 - No auxiliary +12 V power supply on J1 and J4B,
- ST3 = 2-3 - Galvanic insulation or serial ports 1 and 2.

VII.1 Configuring the extension

The *Lite*-485 extension features one set of four switches (SW1), two sets of eight switches (SW2 and SW3), and three jumpers (ST1, ST2 and ST3).

SW1 - Interrupts and input/output address for the extension
The SW1 switch lets you configure the interrupt lines (with the MCX-*Lite*/0 card) and the address ranges used by the extension's 2 serial ports.

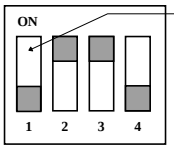
	sw1-1	sw1-2	sw1-3	sw1-4
ON	UNX232 Mode Port 1: 280h Port 2: 288h	IRQ4 port 1 enabled	IRQ3 port 2 enabled	IRQ5 port 1 and 2 enabled
OFF	COM1/COM2 Mode Port 1: 3F8h Port 2: 2F8h	IRQ4 port 1 disabled	IRQ3 port 2 disabled	IRQ5 port 1 and 2 disabled

DIP SW1 - Address and interrupt line selection

Warning: some switch combinations are not valid. For example, you cannot select two interrupt levels for the same port.

- **SW1 switch position in COM1/COM2 emulation:**

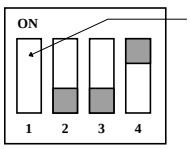
  SW1-1: COM1/COM2 addresses (3F8h/2F8h)
  SW1-2: IRQ4 port 1 enabled
  SW1-3: IRQ3 port 2 enabled
  SW1-4: IRQ5 ports 1 and 2 disabled



You can also set SW1-1 to "ON", but in this case only the IRQ levels are COM1/COM2 compatible.

- **SW1 switch position with ports 1 and 2 using IRQ5 and the address mode of your choice:**

  SW1-1: your choice of addresses
  SW1-2: IRQ4 port 1 disabled
  SW1-3: IRQ3 port 2 disabled
  SW1-4: IRQ5 ports 1 and 2 enabled



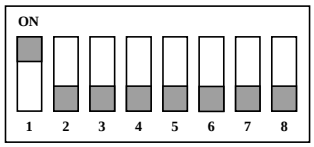
SW1-1 should be set to the desired address range: 3F8h/2F8h or 280h/288h

SW2-SW3 switches - Select RS232, RS422A, RS485 mode and configure serial ports #1 and #2

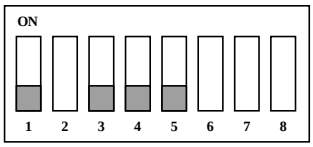
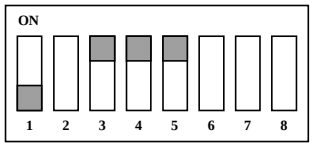
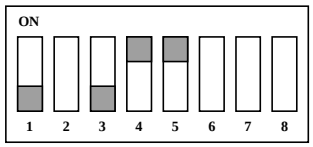
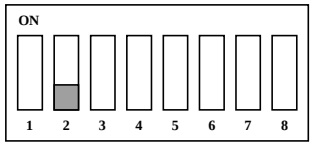
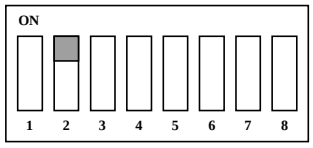
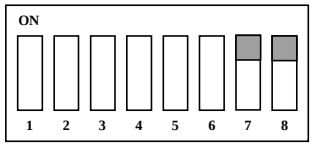
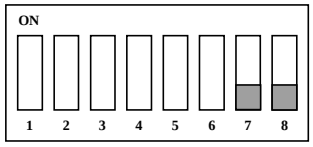
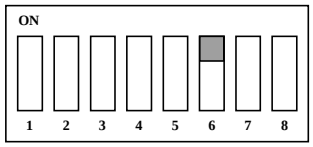
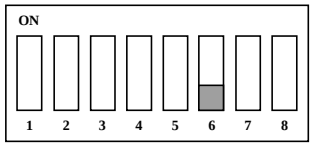
- SW2 configures port #1.

- SW3 configures port #2.

Select RS232D mode for port #1/SW2 and port #2/SW3

	RS232D Mode

Select RS422A or RS485 mode and configure ports # 1/SW2 and # 2/SW3:

	RS422A Mode
	RS485 Mode with ECHO OFF
	RS485 Mode with ECHO ON
	Transmission permanently enabled
	Transmit enable controlled by RTS
	With line polarization
	Without line polarization
	With terminating resistor
	Without terminating resistor

- **ST1 jumper - Parallel port interrupt mode configuration**

  - ST1 in position 1-2: Latched mode.
  - ST1 in position 2-3: Ack. interrupt mode.

- **ST2 jumper - +12V auxiliary power supply on pin #9 of J1 and J4B connectors**

  - ST2 in position 1-2: No +12V auxiliary power supply.
  - ST2 in position 2-3: +12V auxiliary power supply.

- **ST3 jumper - Select galvanic insulation on serial ports #1 and #2**

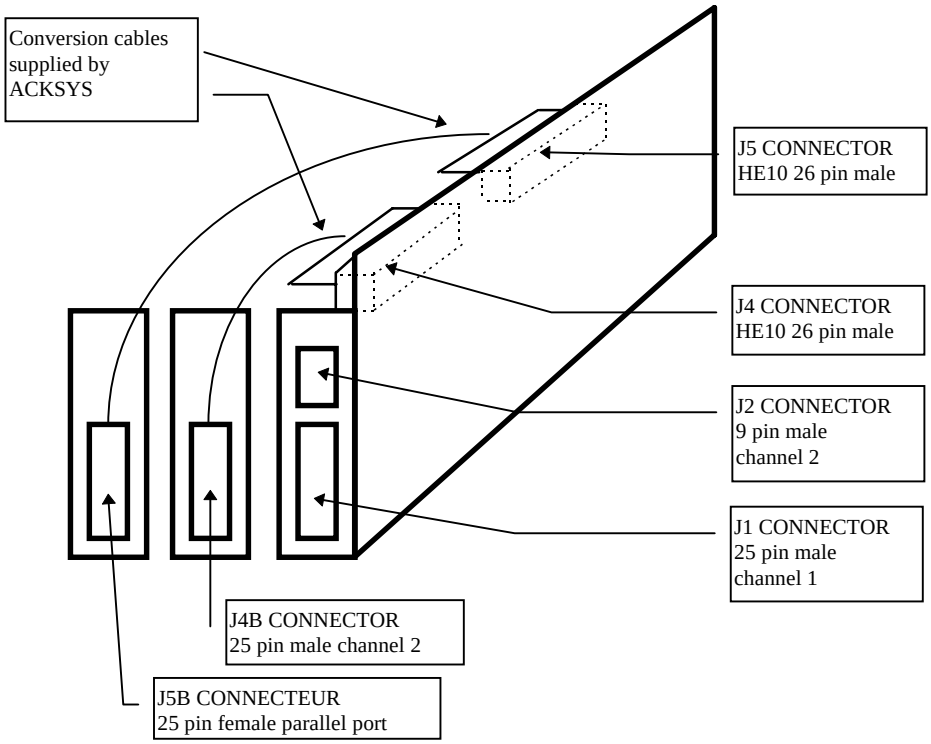
  - ST3 in position 1-2: Without galvanic insulation.
  - ST3 in position 2-3: With galvanic insulation.

Important note:

In RS232D mode with galvanic insulation, only the TXD and RXD signals are converted. The GNDI insulated ground is available on pin #25 of the male SUBD 25 pin connectors (J1 for port #1 and J2 for port #2).
In this case, pins 1 and 7 should not be used. It is therefore impossible to use the 9 pin connector, which has no insulated ground.

VII.2 Installing the MCX-*Lite*/485 card in the PC

You should leave a free slot near the card if you want to replace the 9 pin J2 connector with the 25 pin J4B connector, or if you want to use the parallel port via the J5B connector.



If the SUBD 9 pin connector is replaced by the SUBD 25 pin connector, the 2 serial channels on the card have the same connections.

VII.3 Signals on connectors

The following table describes the signals on each of the of the *Lite*-485 extension's 9 pin and 25 pin connectors.

- **J1 and J4B Connectors**
  These are male SUBD 25 pin connectors. They are attached to serial ports #1 and #2 respectively.

J1 and J4B CONNECTOR - PORT #1 and #2 - Male SUBD 25 pin

Pin #	Signal Direction	Description	EIA RS232D	CCITT V 24 Standard
1	I	PGND		101
2	O	TXD	BA	103
3	I	RXD	BB	104
4	O	RTS	CA	105
5	I	CTS	CB	106
6	I	DSR	CC	107
7	I	GROUND 0V	AB	102
8	I	CD	CF	109
9		+ 12 VDC (200 mA)		
12	O or I/O	- TX or -TX/-RX		
13	O or I/O	+ TX or +TX/+RX		
20	O	DTR	CD	108/2
21	I	-RX		
22	I	RI	CE	125
23	I	+RX		
25		GNDI (Insulated ground)		

I: Input signals
O: Output signals

- RS422A uses the +RX(23),-RX(21) and +TX(13),-TX(12) signals.
- RS485 uses the +TX/+RX(13) and -TX/-RX(12) signals.
- RS232D uses the TXD(2) and RXD(3) signals.

- **J2 Connector**
  This male SUBD 9 pin connector is attached to serial port #2.

J2 CONNECTOR - PORT #2 - Male SUBD 9 pin

Pin #	Signal Direction	Description	EIA/TIA 574
1	I	DCD	109
2	I	RXD	104
3	O	TXD	103
4	O	DTR	108/2
5		GND	102
6	I	DSR	107
7	O	RTS	105
8	I	CTS	106
9	I	RI	125

I: Input signals
O: Output signals

The RS422A and RS485 signals are not available on this connector.

Warning: this connector can only be used by serial port #2 in non-insulated RS232D mode.

VII.4 Electrical and mechanical specifications

* Transmission type	Asynchronous, full duplex, half duplex and simplex.
* Interface type	- EIA RS232D/CCITT V24, EIA 574 - EIA RS422A - EIA RS485/CCITT V11
* Signals converted with galvanic insulation	RX and TX
* Control signal	RTS controls transmit enable. - RTS at 0: transmitter enabled. - RTS at 1: transmitter disabled.
* Signals without galvanic insulation	RTS, DTR, CTS, DCD, RI and DSR
* Maximum rate	115.2 Kbps (only in RS422-RS485)
* Maximum voltage in common mode (RS422-RS485)	± 7V
* Maximum capacity in RS422 (limited by the EIA standard)	10 receivers
* Maximum capacity in RS485 (Limited by the EIA standard)	32 transmitters/receivers
* Maximum transmission distance (RS422-RS485), (limited by the EIA standard; depends on the transmission speed and the type of cable used)	1200 m for a gauge 24 cable (0.22 mm^2) and with a capacitance of 50 pF/m between conductors
* Type of cable to use (RS422A-RS485)	Gauge 24 twisted pair(s), 50 pF/m, nominal impedance 120 Ω. In very noisy industrial environments, a grounded shield is required. Capacitance between grounded shield and conductors: 75pF/m
* Maximum distance for RS232D transmission	16.5 m
* Protection against transiert voltage surges (RS422A-RS485)	Breakdown voltage per peak: - ± 7V in common mode. - ± 14V in differential mode. - Absorption capacity: 0.3 kW during 1 mS.

* Protection against transient voltage surges (RS232D)	By transils, Breakdown voltage: - ± 25V in common mode. - Absorption capacity: 0.3 kW during 1 mS.
* Protection against electrostatic discharges in accordance with EIC 801-2 (RS422A-RS485 and RS 232D)	The system exceeds the upper limit of the standard (level 4 15 kV maximum voltage). Furthermore, the standard only specifies single discharges applied on the external housing and not directly on the signals. - Single discharge test: > 21 kV. - 20 Hz impulse test: duration 1 S ≥ 20 kV.
* Galvanic isolation (1 minute test voltage) RS422A-RS485 and RS232D	- Optocouplers and dc/dc converter. - 2.5 kV_{rms} & 3 $kV_{dc.}$ insulation - 1200 V_{rms} mini.
* Immunity to transients (RS422A-RS485 and RS232D with insulation)	10000 V/µs at Vcm = 1000 V.
* Temperature range	- from -5°C to +65°C.
* Humidity	- from 0 to 95% RH, without condensation.

Electrical specifications of the *Lite*-485 extension

POWER CONSUMPTION	
+ 5 V DC	±12 V DC
0.25 A max / 1.25 W	18 mA max / 216 mW

Electrical and mechanical specifications of the MCX-*Lite*/485 card

POWER CONSUMPTION			DIMENSIONS	OPERATING CONDITIONS		
+ 5 V DC	+ 12 V DC	- 12 V DC	Length x Width	Relative humidity (non-condensing)	Temperature	Storage
1.73 A max / 8.65 W	18 mA max / 216 mW	18 mA max / 216 mW	340mm x115 mm	95% to +25°C	-5 to +65°C	-25 to +70°C

The dimensions do not include the attachment bar and the two ISA connectors.

Power consumption calculations are based on an MCX-*Lite*/485 card with an 80386 SX 25 Mhz processor, 4 Mbytes RAM and 2 serial channels programmed in RS232A mode with a resistance of 90 Ohms.

VII.5 Programming

This information is provided only for writing programs that are internal to the card.

VII.5.1 Input/output ports on the *Lite*-485 extension

The base addresses for the serial channels depend on the position of the SW1-1 switch.

SW1-1	PORT 1	PORT 2
ON	280h	288h
OFF	3F8h	2F8h

Each serial ports occupies 8 input/output addresses starting at the associated base address. The appendix on the 16C550 provides all the characteristics of the STARTECH 16C552, with which the 16C550 is fully compatible.

The parallel port occupies 8 input/output addresses starting at the base address of 378h, and uses the IRQ7 interrupt (LPT1).

VII.5.2 Enabling interrupts

You may control interrupts at four levels:

* via the channel interrupt register, evaluated for all interrupt types.
* globally for a channel, via the OUT2 bit in its MODEM control register.
* via the 8259 controller on the MCX-*Lite*/0 card, by managing the selected interrupt line.
* using the processor's CLI/STI instructions.

Warning: the 8259 also uses IRQ7 to indicate a "SPURIOUS INTERRUPT" condition.

VII.5.3 Baud rate generator

All the baud rate generators use a common 1.8432 Mhz clock. The transmit and receive clocks are interconnected.

CONTENTS

VIII. THE LITE-104 EXTENSION VIII-1

VIII.1 CONFIGURING THE EXTENSION VIII-2

VIII.2 SIGNALS ON CONNECTORS VIII-6

VIII. THE LITE-104 EXTENSION

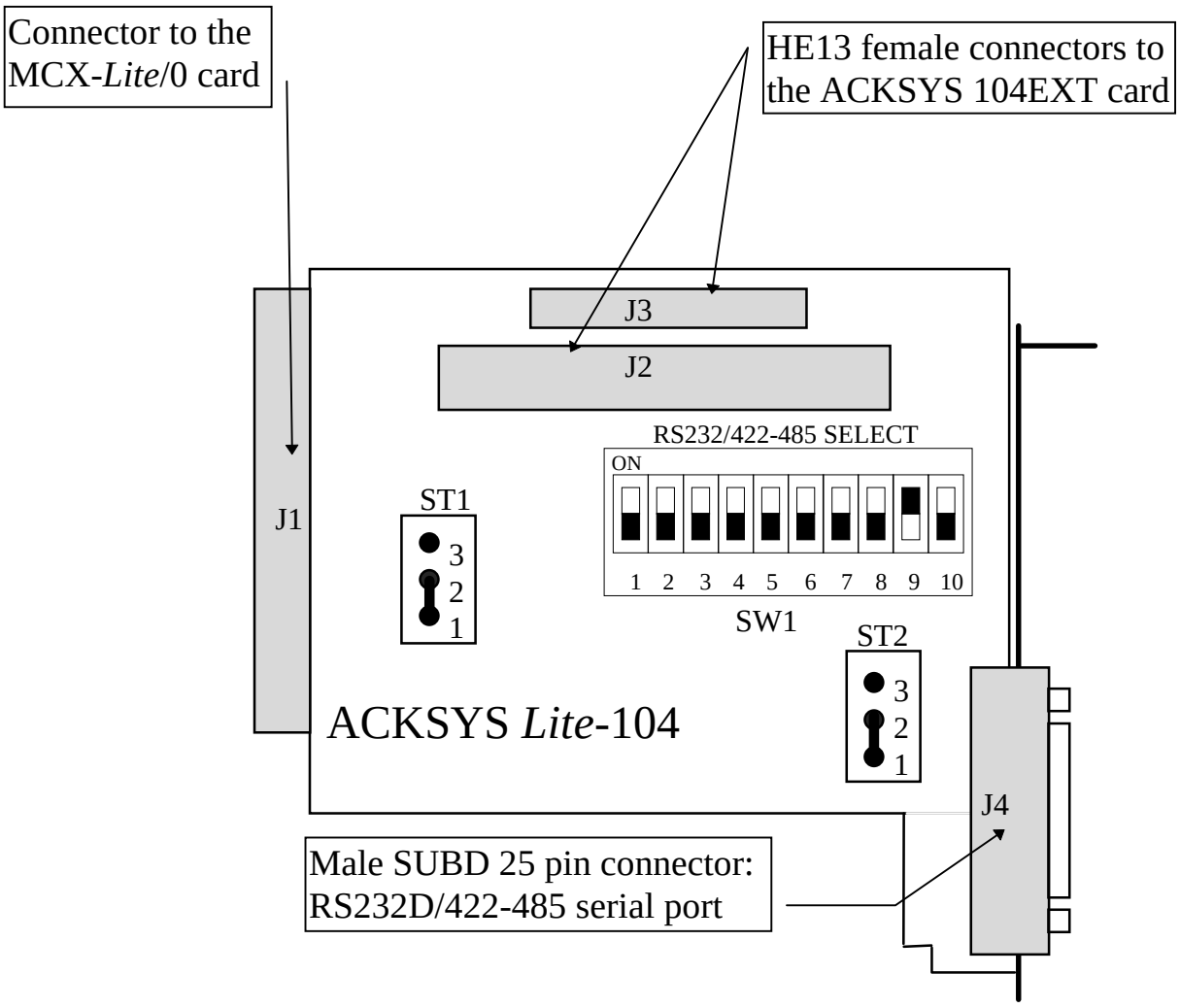
When attached to the MCX-*Lite*/0 card, the *Lite*-104 extension adds an asynchronous RS232/RS422/RS485 serial port (16C550 UART) as well as two PC-104 slots.

Its installation is the same as for all the options of the Lite family: simply connect one end of the extension to the MCX-*Lite*/0 card.

The *Lite*-104 extension includes two printed circuits:

- the main *Lite*104 circuit contains the serial interface,
- the extension circuit (104EXT) lets you attach 1 or 2 PC-104 cards.

Basic printed circuit on the *Lite*104



Factory settings .	ST1 in position 1-2 - Serial port on COM1 ST2 in position 1-2 - Pin 9 of J4 not connected SW1- RS232D Serial port

VIII.1 Configuring the extension

- **ST1 jumper - Configure the serial port in COM1 or COM2 mode**

  The jumper at ST1 configures the Lite-104 extension's serial port mode:

Position 1-2	COM1 Mode	Address 3F8h	Interrupt IRQ4
Position 2-3	COM2 Mode	Address 2F8h	Interrupt IRQ3

- **ST2 jumper - (+12V on pin 9 of the J4 SUB D25 connector)**

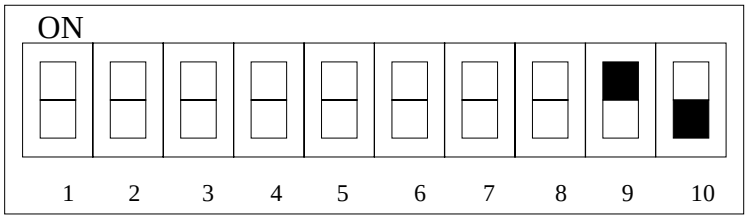
  The jumper at ST2 connects or disconnects the + 12V signal to pin 9 on the SUB D 25 pin connector (this pin may be used to power external devices, up to 200 mA).

  - Position 1-2 Pin 9 not connected
  - Position 2-3 Pin 9 connected to +12VDC

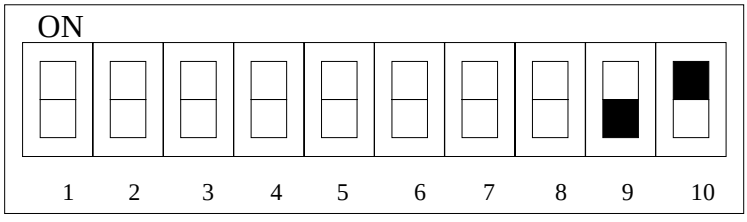
- **SW1 - Configure the serial port's RS232, RS422 and RS485 modes**

  The set of switches at SW1 configures the electrical serial interface of the Lite-104 extension.

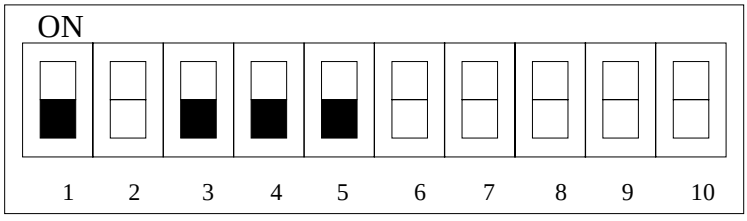
Standard Configurations



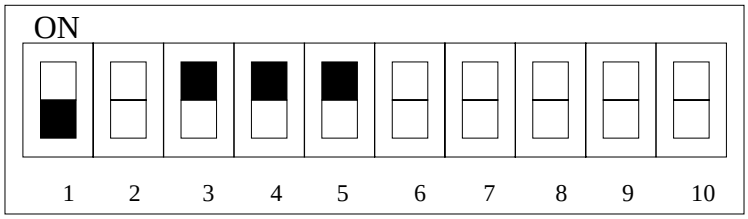
RS232 mode



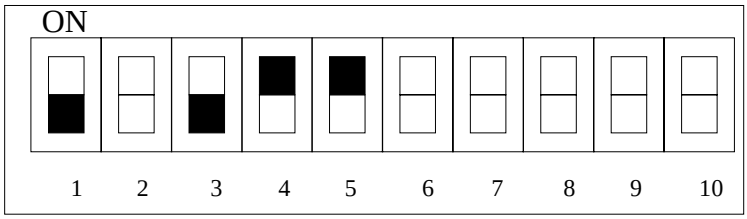
RS422A/RS485 mode



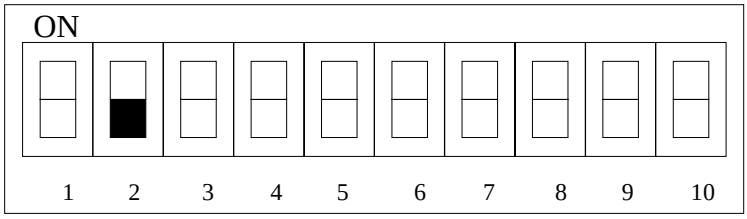
RS422A mode



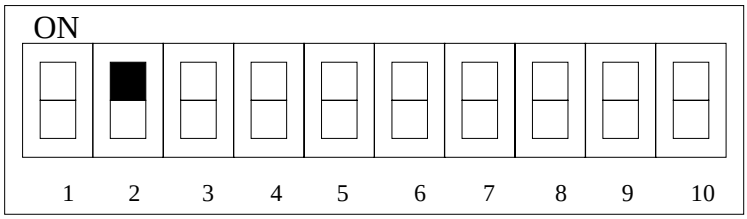
RS485 mode with ECHO OFF



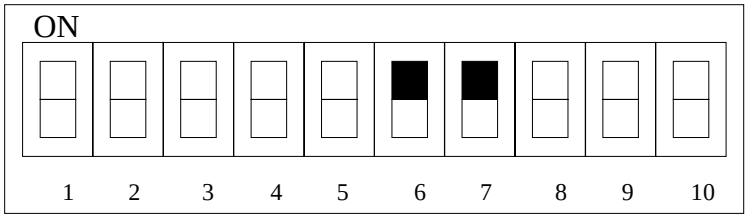
RS485 mode with ECHO ON



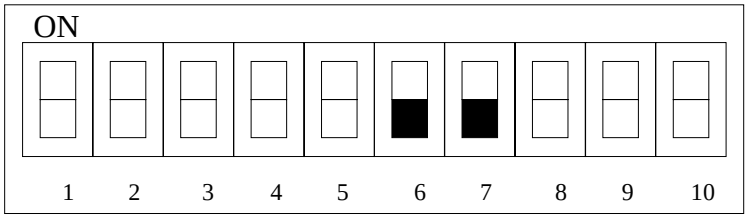
Permanent transmit enable



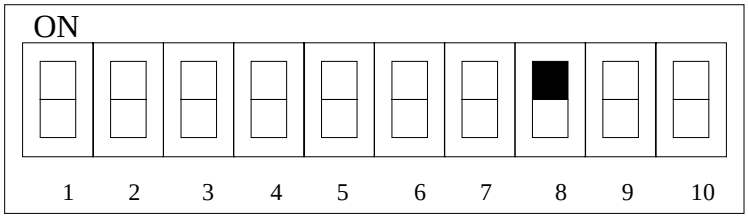
Transmit enable controlled by RTS



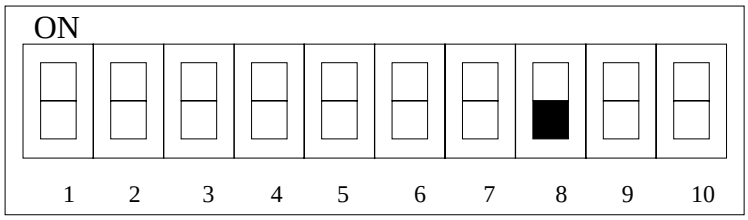
With line polarization



Without line polarization

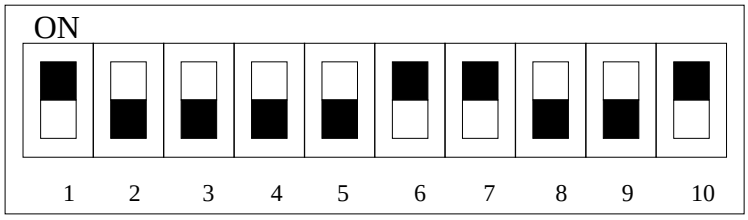


With terminating resistor

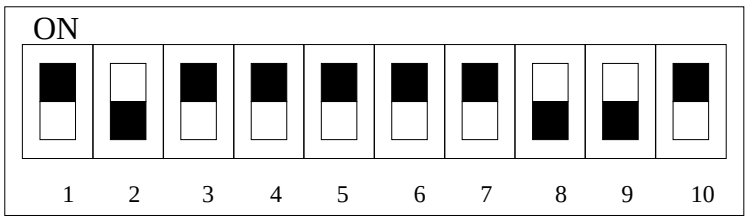


Without terminating resistor

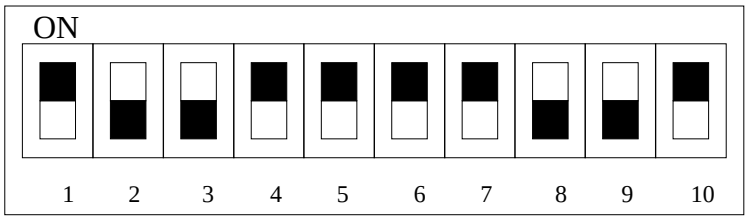
SPECIAL CONFIGURATIONS
TRANSMIT ENABLE CONTROLLED BY TXD



RS422A mode (Slave)



RS485 mode with ECHO OFF

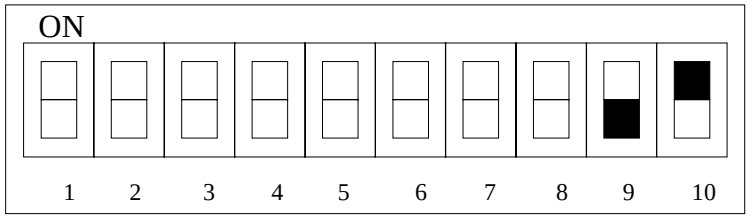


RS485 mode with ECHO ON

⇒ **Limitations related to transmit enable by TXD**

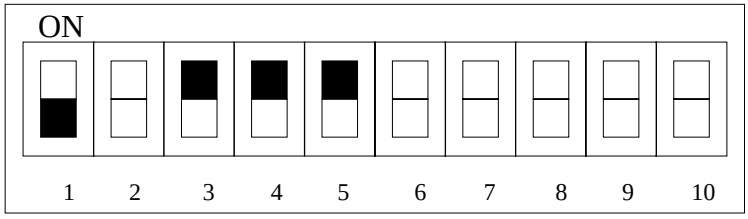
- Limit the speed of communications to 56 Kbits/second.
- Limit the number of RS485 interfaces to 20, with a maximum length of 200 meters.
- Do not use line terminating resistors.
- Provide line polarization on the Lite-104 card's serial port (only one polarization per line, SW1-6 & SW1-7 in ON position).
- Avoid noisy environments.
- Use a grounded braided shielded cable (recommended).

Configuration example



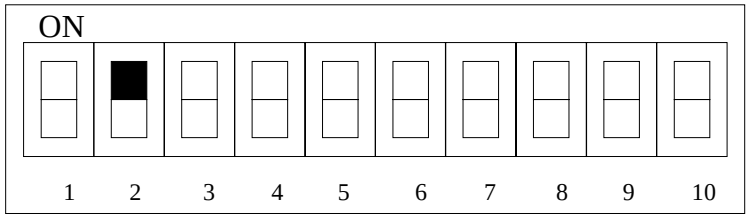
RS422/485 mode

+



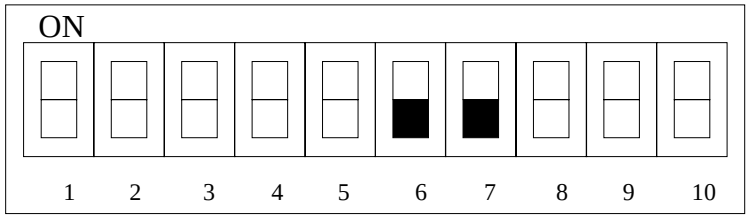
RS485 mode with ECHO OFF

+



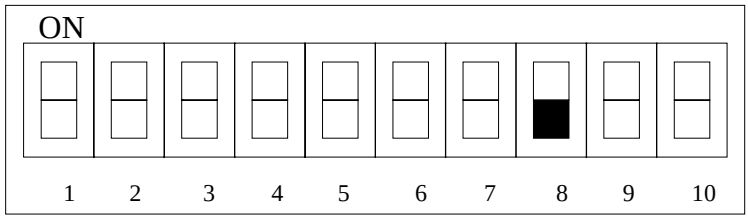
Transmit enable controlled by RTS

+

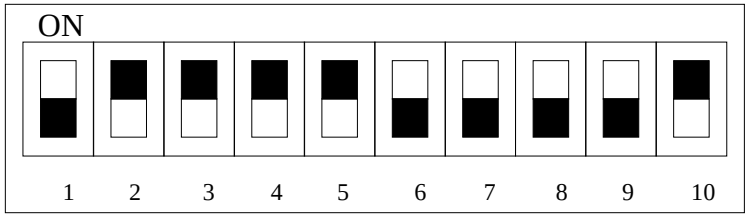


Without line polarization

+



Without terminating resistor



=

VIII.2 Signals on connectors

The Lite-104 extension card includes a male SUB D 25 pin connector (J4) that groups the serial communications port's RS232, RS422 and RS485 signals.

The following table describes the signals on this connector.

- **J4 Connector**

1	PGND
2	TXD
3	RXD
4	RTS
5	CTS
6	DSR
7	GND
8	xxxxxx
9	+12VDC
10	xxxxxx
11	xxxxxx
12 [1]	-TX [1]
13 [1]	+TX [1]

14	xxxxxx
15	xxxxxx
16	xxxxxx
17	xxxxxx
18	xxxxxx
19	xxxxxx
20	DTR
21	-RX
22	RI
23	+RX
24	xxxxxx
25	xxxxxx

xxxxxx: Signals not used.

[1] In RS485 mode, you must use pins 12 (-TX/-RX) and 13 (+TX/+RX).

Signals on the PC-104 connector

The PC-104 connector generally repeats the signals of the 8/16 bits ISA bus. It uses an HE13 connector instead of the traditional PC edge connectors:

- **J2 Connector**

A1	-IOCHK
A2	SD7
A3	SD6
A4	SD5
A5	SD4
A6	SD3
A7	SD2
A8	SD1
A9	SD0
A10	IOCHRDY
A11	AEN
A12	SA19
A13	SA18
A14	SA17
A15	SA16
A16	SA15

A17	SA14
A18	SA13
A19	SA12
A20	SA11
A21	SA10
A22	SA9
A23	SA8
A24	SA7
A25	SA6
A26	SA5
A27	SA4
A28	SA3
A29	SA2
A30	SA1
A31	SA0
A32	GND

B1	GND
B2	RESETDRV
B3	+5VDC
B4	IRQ9 (*)
B5	-5VDC
B6	DRQ2
B7	-12VDC
B8	-ENDXFR
B9	+12VDC
B10	(KEY)
B11	-SMEMW
B12	-SMEMR
B13	-IOW
B14	-IOR
B15	-DACK3
B16	DRQ3

B17	-DACK1
B18	DRQ1
B19	-REFRESH
B20	CLK
B21	IRQ7
B22	IRQ6
B23	IRQ5
B24	IRQ4
B25	IRQ3
B26	-DACK2
B27	T/C
B28	BALE
B29	+5VDC
B30	OSC
B31	GND
B32	GND

- **J3 Connector**

C0	GND
C1	SBHE
C2	LA23
C3	LA22
C4	LA21
C5	LA19
C6	LA20
C7	LA18
C8	LA17
C9	-MEMR
C10	-MEMW
C11	SD8
C12	SD9
C13	SD10
C14	SD11
C15	SD12
C16	SD13
C17	SD14
C18	SD15
C19	(KEY)

D0	GND
D1	-MEMCS16
D2	-IOCS16
D3	IRQ10 [2]
D4	IRQ11
D5	IRQ12
D6	IRQ15
D7	IRQ14
D8	-DACK0 [2]
D9	DRQ0 [2]
D10	-DACK5
D11	DRQ5
D12	-DACK6
D13	DRQ6
D14	-DACK7
D15	DRQ7
D16	+5VDC
D17	-MASTER [2]
D18	GND
D19	GND

Note for installing PC-104 extension cards

As discussed previously in this document, you may attach two PC-104 format daughter cards to the Lite-104 extension card.

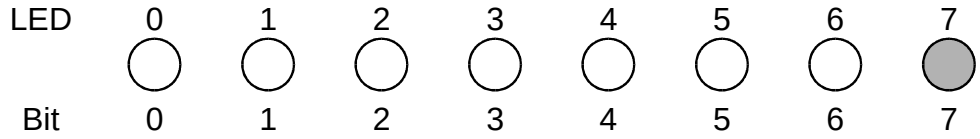
In order to avoid short circuits and to avoid wasting slots in your machine, we recommend that you cut the transfer pins for mounting a "piggy-back" card on the last daughter card.

[2] The IRQ9, IRQ10, DRQ0, -DACK0 and -MASTER signals are not available on the PC-104 connector because they are used for the MCX-*Lite* card's internal operations.

Appendix A: AUTOMATIC POWER ON SELF-TEST

When you power on the system, the MCX card performs several tests to verify that its peripherals are in working order.

The results of these tests are displayed in a visual code, so you can identify the error immediately.
This code is displayed on the set of eight LEDs in binary format. The codes have the following meanings:



Code 01h ..... CPU flags register error.
Code 02h ..... CPU register error.
Code 03h ..... BIOS memory checksum error.
Code 04h ..... DMA controller error.
Code 05h ..... System TIMERS error.
Code 06h ..... Error when testing first 64 K or incorrect memory configuration.
Code 07h ..... Error when testing first 64 K.
Code 08h ..... INT controller error.
Code 09h ..... Unexpected INT detected.
Code 0Ah ..... No TIMER interrupt.
Code 0Bh ..... CPU already in protected mode.
Code 0Ch ..... Error in DMA page register.
Code 0Dh ..... No memory refresh.
Code 0Eh ..... 8042 micro-controller error.
Code 0Fh ..... Cannot enter protected mode.
Code 10h ..... GDT or IDT register error.
Code 11h ..... LDT register error.
Code 12h ..... Task register error.
Code 13h ..... LSL instruction error.
Code 14h ..... LAR instruction error.
Code 15h ..... VERR / VERW error.
Code 16h ..... Error on address line A20.
Code 17h ..... Unexpected exception.
Code 18h ..... Shutdown during memory test.
Code 19h ..... Copyright checksum error.
Code 1Ah ..... Parameter checksum error.
Code C0h ..... Memory test error.
Code C1h ..... IO/CHECK signal error.
Code C2h ..... "Watchdog timeout".
Code C4h ..... "Bus timeout".

The following errors are only significant in "MCC emulation" mode.

Code 81h ..... SCC 85C30 error.
Code 82h ..... Dual-ported memory error.
Code 83h ..... Unexpected TRAP error.
Code 84h ..... Memory buffer error.
Code 85h ..... Firmware checksum error.
Code 86h ..... Lithium battery error.
Code 87h ..... MCX to PC interrupt error.
Code 88h ..... "Watchdog" error.
Code 89h ..... FIFO access error.
Code 8Ah ..... SCC error during RX and TX test loop.
Code 8Bh ..... SCC error during high-speed DMA test.
Code 8Ch ..... General protection fault.
Code 8Dh ..... Memory size error.
Code 8Eh ..... NMI interrupt received.

Note that during the test, LEDs 0 through 7 are turned on successively. They are turned off by a CPU "HALT" if an error occurs. The error code is then displayed.

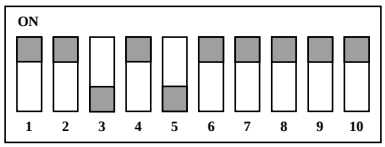
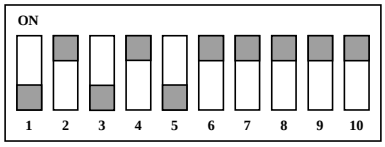
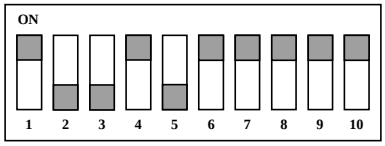
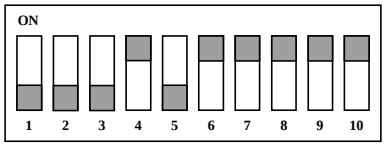
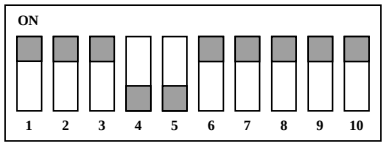
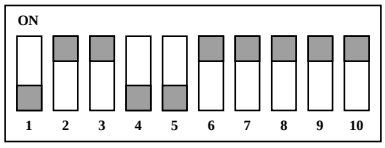
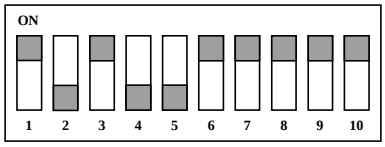
When the test has been correctly executed in MCC emulation mode, LEDs 0 through 7 light quickly from bottom to top, then in the opposite direction to indicate that the card is waiting for its start code (RUN 01 or RUN 02).

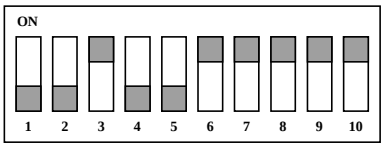
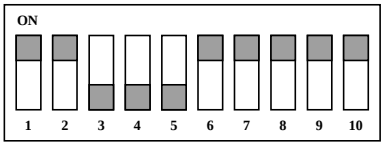
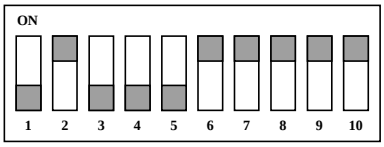
When the test has been correctly executed in MCXDOS mode, LEDs 0 through 7 are turned off to indicate that the card is waiting for its start code (RUN 99).

If one of the errors listed above is encountered during the card's power on self-test, you should contact your dealer, who will have it repaired as quickly as possible.

Appendix B : SW3 SWITCH SETTINGS

The table below illustrates the most common settings for the set of switches at SW3 on MCX-00 and MCX-*Lite*/0 motherboards.

BASE ADDRESS (SEGMENT)	SW3 CONFIGURATION
A000	
A800	
B000	
B800	
C000	
C800	
D000	

D800	
E000	
E800	

Appendix C: 16C550 SPECIFICATIONS

The communications devices integrated on the *Lite*-UNX ((16C554 - 4 channel 16C550) and the Lite-485 (16C552 - 2 channel 16C550) are fully compatible with the basic 16C550 communication device.

General Features

* Asynchronous serial communications.
* CMOS Technology.
* Designed for easy interfacing with the most popular microprocessors (80286, 80386 , 80486, etc.).
* Emulates 16C450 and 8250 modes.
* Independent control of the transmit, receive line status and data set interrupts.
* Programmable baud rate generator.
* Independent receiver clock input.
* 16 byte FIFO receive and transmit buffer.
* Fully programmable data format:
  - 5,6,7,8 bits per character,
  - Even, odd or no parity,
  - 1,1+1/2,2 stop bits.
* False start bit detection.
* Complete status reporting capabilities.
* Tri-state TTL drive and bi-directional data bus.
* Detects and generates "Breaks".
* Internal loop testing available to detect hardware failures.
* Error detection: "Break", parity, overload, frame.
* Priority-based interrupt arbitration system.
* Single +5V power supply.

This component is used to serialize data on the transmitter and to de-serialize data on the receiver.

The following serial transmit/receive data format is used:
1 start bit,
+ from 5 to 8 data bits (transmitted from least- to most-significant bit),
+ 1 parity bit, if programmed,
+ 1 bit + 1/2 bit (5 data bits) or 2 stop bits.

The maximum recommended transmission rate is 115,200 bits/second.

The internal registers let programmers use several types of interrupts, various character formats, and simplified management of "Modem" signals. You can read the 16C550 status bits at any time, and modify them dynamically if required.

The 16C550 includes a programmable baud rate generator than can divide an external frequency from a quartz or a TTL signal by a factor of 1 to 2^{16} -1.

The asynchronous communication unit can operate in both "Polling" and interrupt modes.

Addressing registers

The table below illustrates the various registers selected according to the address configurations:

DLAB	A2	A1	A0	Register
0	0	0	0	Receive register (read) Transmit register (write)
0	0	0	1	Interrupt authorization
X	0	1	0	Interrupt identification
X	0	1	1	Line control
X	1	0	0	Modem control
X	1	0	1	Line status
X	1	1	0	Modem status
X	1	1	1	Not used
1	0	0	0	Dividing factor (LSB)
1	0	0	1	Dividing factor (MSB)

Note:
Bit 7 of the line control register is the DLAB bit. The program must set this bit to 1 in order to access the divisor latches of the baud generator.

Line control register (LCR)

- **Bits 0 and 1**:
  These two bits specify the number of bits in each received or transmitted character, as indicated in the table below:

Bit 1	Bit 0	Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- **Bit 2**:
  This bit specifies the number of stop bits at the end of each character received or transmitted by the 16C550.
  - Bit 2 = 0 ⇒ 1 stop bit
  - Bit 2 = 1 ⇒ 1+1/2 stop bit for 5 bits, or
    ⇒2 stop bits for 6,7,8 bits.

- **Bit 3**:
  This bit enables or disables the parity bit.
  - Bit 3 = 1 ⇒ 1 parity bit generated
  - Bit 3 = 0 ⇒ No parity

- **Bits 4 and 5**:

Bit 5	**Bit 4**	**DESCRIPTION**
0	0	Odd parity
0	1	Even parity
1	0	Parity bit forced and controlled at 1
1	1	Parity bit forced and controlled at 0

- **Bit 6**:
  When bit 6 is at logic level 1, the 16C550 generates a "Break" on the line until bit 6 is set to 0.

- **Bit 7**:
  DLAB Bit: When set to 1, this bit lets you access the divisor latches of the baud generator. It must be set to 0 to access the interrupt, transmit and receive registers.

Baud rate generator

The 16C550 features a programmable baud rate generator able to divide an input frequency from a quartz or a TTL signal by a factor of 1 to 2^{16}-1.

The baud rate generator's output frequency must be 16 times greater than the transmit-receive rate. Two 8 bit registers let you write the dividing factor's most significant byte and least significant byte.

The table below illustrates the use of the baud rate generator based on a 1.8432 Mhz quartz:

Rate	Decimal factor	Hex factor	% error
50	2304	900	0
75	1536	600	0
110	1047	417	0.026
134.5	857	359	0.058
150	768	300	0
300	384	180	0
600	192	C0	0
1200	96	60	0
1800	64	40	0
2000	58	3A	0.69
2400	48	30	0
3600	32	20	0
4800	24	18	0
7200	16	10	0
9600	12	0C	0
19200	6	06	0
38400	3	03	0
56000	2	02	2.86
57600	2	02	0
115200	1	1	0

Line status register (LSR)

The line status register provides the CPU with all the information concerning the data transfer. The meaning of each bit is described below:

- **Bit 0:**
  This bit indicates that data is ready in the receive register, or that data has been transferred to the FIFO receive buffer. It is automatically reset to 0 when you read the character or the FIFO buffer.
- **Bit 1:**
  It indicates that the character in the receive register has been overwritten by another character before the first character was read by the CPU. In FIFO mode, this bit indicates a FIFO buffer overflow. This bit is reset to 0 when you read the line status register.
- **Bit 2:**
  This bit indicates a parity error. The character received did not have the correct parity. This bit is reset to 0 when you read the line status register.
  In FIFO mode, this bit indicates that the character currently at the top of the FIFO buffer has a parity error.
- **Bit 3:**
  It indicates a frame error: the stop bit following the last data bit or parity bit was detected with a value of 0. This bit is reset to 0 when you read the line status register.
  In FIFO mode, this bit indicates that the character currently at the top of the FIFO buffer has a frame error.
- **Bit 4:**
  This bit tells the CPU that a "Break" has been detected on the line (all bits at 0 for a period greater than one character).
  In FIFO mode, this bit indicates that the character currently at the top of the FIFO buffer was generated by the "Break" signal.
  Note: If you wish, the events associated with bits 0, 1, 2 and 3 may generate a "receive" interrupt when they are detected.
- **Bit 5:**
  This bit indicates that the transmit unit is ready to receive a character from the CPU. Furthermore, this bit may also generate a transmit interrupt if the interrupt register has been programmed correctly. In FIFO mode, it indicates that the FIFO transmit buffer is empty: this bit is reset to zero as soon as at least one character is present in the FIFO buffer.
- **Bit 6:**
  When set to 0, this bit indicates that the transmitter is currently functioning. It is automatically reset to 1 when the receive register and the transmission shift register are empty at the same time.
  In FIFO mode, when set to 1, this bit indicates that the FIFO transmit buffer and the transmit shift register are totally empty.
- **Bit 7:**
  In 16C450 mode, this bit always equals 0. In FIFO mode, it indicates that the FIFO receive buffer contains at least one incorrect character. This bit is automatically reset to zero when you read the line status register.

The FIFO control register (FCR)

This register can be read under the name of the interrupt identification register. You can also write to this register. It lets you control the FIFO buffer:

* Enable FIFO mode.
* Clear the FIFO buffer.
* Select the FIFO buffer receive mode.

These controls are performed as follows:

- **Bit 0:**
  When set to logic level 1, this bit (FCR0) enables the FIFO mode for both transmit and receive operations. If set to 0, FIFO mode is disabled, and all the characters in the FIFO buffer are erased.
  When going from 16C450 mode to the 16C550 FIFO mode or vice versa, all data in the FIFO buffer is erased.
  This bit must be set to 1 in order to program the other bits in this register.
- **Bit 1:**
  When set to 1, this bit (FCR1) erases all the data in the FIFO receive buffer; it also resets the character counter to zero. The shift register is not erased, however. The FCR1 bit is automatically reset to zero after being used.
- **Bit 2:**
  When set to 1, this bit (FCR2) erases all the data in the FIFO transmit buffer; it also resets the character counter to zero. The shift register is not erased, however. The FCR2 bit is automatically reset to zero after being used.
- **Bit 3:**
  This bit (FCR3) concerns the TXRDY and RXRDY pins, which are not used in this card. These two signals may be used to trigger DMA cycles.
- **Bits 4, 5:**
  Bits 4 and 5 (FCR4 and FCR5) are reserved for future use.
- **Bits 6, 7:**
  These two bits (FCR6 and FCR7) are used to tell the receive FIFO that it should generate a FIFO interrupt.
  Use the table below to make this selection:

Bit 7	Bit 6	Number of characters in the FIFO buffer
0	0	1
0	1	4
1	0	8
1	1	14

The interrupt identification register (IIR)

This register's address is the same as that of the 16C450 (note: it is located at the same address as the FIFO control register). The bits in this register have the following meaning:

- **Bit 0:**
  This bit may be used in "Polling" mode. When set to 1, it indicates that an interrupt condition is active. The identification register contents may then be used as a pointer to the appropriate interrupt routine.
- **Bits 1 and 2:**
  These two bits in the identification register may be used to determine the source of the interrupt as illustrated in the table below.
- **Bit 3:**
  In FIFO mode, this bit is set to 1 to indicate that a "Timeout" interrupt is waiting.
- **Bits 4 and 5:**
  These two bits are always at logic level zero.
- **Bits 6 and 7:**
  These two bits are set to 1 when the FCR0 bit in the FIFO control register equals 1.

The table below summarizes the various states that may cause interrupts, and indicates how to reset them to zero.

Interrupt identification table:

Bit 3	Bit 2	Bit 1	Bit 0	Priority	Source	To reset to 0
0	0	0	1		None	
0	1	1	0	1st (High)	Overflow Parity Frame Break	Read the line status register
0	1	0	0	2nd	Character ready FIFO buffer ready	Read the receive register or the FIFO register
1	1	0	0	2nd	FIFO timeout	Read the receive register or the FIFO register
0	0	1	0	3rd	Transmitter empty	Write a character or read the IIR
0	0	0	0	4th (Low)	CTS DSR RING RLSD	Read modem status register

Interrupt enable register (IER)

The only difference between the 16C450 and the 16C550 models concerns bit 0 of this register. It enables receive interrupts, and also enables receive "timeout" interrupts.

FIFO interrupt management

A. When both FIFO receive interrupts and the receiver are enabled, a receive interrupt is triggered as follows:
The receive interrupt is sent to the CPU when the number of characters in the FIFO buffer reaches the number programmed in the FIFO control register (bits 6 and 7). The interrupt and the corresponding bit in the interrupt identification register are reset to zero as soon as the number of characters contained in the buffer falls below the programmed value.

Note that the status interrupt has a higher priority than the receive character interrupt. The character ready bit is set to 1 as soon as a character is transferred from the shift register to the FIFO buffer; this bit is reset to 0 as soon as the FIFO buffer has been emptied.

A. When both FIFO receive interrupts and the receiver are enabled, a "Timeout" interrupt is triggered as follows:
A "Timeout" interrupt is generated when the following conditions are detected simultaneously:
* The FIFO buffer contains at least one character.
* The time required to receive the most recent character was greater than the time required to receive the four previous characters.
The time the CPU required to read the most recent character is greater than the time required to receive the four previous characters. This represents a time of 160 ms at 300 bits/second (with 12-bit characters) to generate a "Timeout" interrupt. When the "Timeout" interrupt is generated, reading a character in the FIFO buffer resets the timer to zero.

In normal operations, the "timeout" counter is automatically reset to zero each time a character is received in or taken from the FIFO buffer.

C. When the FIFO transmit interrupt is enabled, transmit interrupts are triggered as follows:
An empty FIFO transmit interrupt is triggered when the FIFO buffer is completely empty. This interrupt is automatically reset to zero when a new character is written to the FIFO buffer. Up to sixteen characters may be sent to the FIFO buffer when the interrupt is received.

The FIFO "timeout" and FIFO receive interrupts have the same priority as the receive character interrupt. The empty FIFO transmit interrupt has the same priority as the transmit character interrupt.

"Polling" mode interrupt management

When interrupts are not enabled, you can control the FIFO buffer in "polling" mode. Since the transmitter and the receiver are controlled separately, only one of the two may be used in "polling" mode.

In "polling" mode, the programmer must test the transmit and receive units using the line status register.

Bit 0 of the line status register is set to 1 as long as at least one character remains in the FIFO receive buffer.
Bits 1 through 4 of the line status register indicate any errors that might have arisen. The error management must be performed as when during an interrupt.
Bit 5 of the line status register indicates that the FIFO transmit buffer is empty, while bit 6 indicates that the FIFO transmit buffer and the transmit shift register are empty.
Finally, bit 7 indicates that the FIFO receive buffer contains at least one incorrect character.

Modem control register

This 8 bit register controls the Modem interface. The bits in this register have the following meanings:

- **Bit 0:**
  This bit controls the "Data terminal ready DTR" output.
  - Bit 0 = 0 ⇒ DTR/ logic level 1.
  - Bit 0 = 1 ⇒ DTR/ logic level 0.
- **Bit 1:**
  It controls the "Request to send RTS" output.
  - Bit 0 = 0 ⇒ RTS/ logic level 1.
  - Bit 0 = 1 ⇒ RTS/ logic level 0.
- **Bit 2:**
  This bit controls the "OUT1/" output, it is not used in the *Lite*-UNX extension.
- **Bit 3:**
  It controls the "OUT2/" output, used to enable the interrupt line amplifier. This bit must be set to 1 in order to use the *Lite*-UNX extension with interrupts.
- **Bit 4:**
  This bit initiates the 16C550's internal diagnostic mode. Information flows directly from the transmitter to the receiver. The DTR/, RTS/, OUT1/ and OUT2/ signals are connected internally to the Modem inputs, so the circuit's internal functions and registers may be tested. In the "Diagnostic" mode, the receiver-transmitter interrupts are fully operational.
- **Bits 5-7:**
  These bits are always forced to logic level 0.

The modem status register

This 8 bit register informs the CPU of the status of the Modem control lines, or of the peripherals connected to the communication line. The bits in this register are set to 1 when they change state, and are reset to 0 by reading this register.

- **Bit 0:**
  This is the "Delta clear to send DCTS" bit. It indicates that the CTS/ input was modified since the last CPU read.

- **Bit 1:**
  This is the "Delta data set ready DDSR" bit. It indicates that the DSR/ input has changed state.

- **Bit 2:**
  This bit indicates that the "Ring indicator RI" input has gone from logic level 1 to logic level 0.

- **Bit 3:**
  This is the "Delta received line signal detector DRLSD" bit. It indicates that the RLSD/ input has changed state.

Note: As soon of one of the bits 0, 1, 2 or 3 changes to logic level 1, a "Modem Status" interrupt is generated.

- **Bit 4:**
  This bit is the reverse image of the CTS/ input bit.

- **Bit 5:**
  This bit is the reverse image of the DSR/ input bit.

- **Bit 6:**
  This bit is the reverse image of the RI/ input bit.

- **Bit 7:**
  This bit is the reverse image of the RLSD/ input bit.

Appendix D: 85C30 FEATURES

Warning

Those wishing to program the MCX-XX and the MCX-*Lite*/S cards should obtain the complete documentation of the 85C30 under the following reference:

> Am8530H/Am85C30 (Advanced Micro Devices)
> Serial Communication Controller
> Technical Manual

The information provided below provides beginners with general information to help them better understand the complete technical documentation.

General features of the SCC 85C30

The SCC 85C30 features two independent "full duplex" communication channels with programmable dividers that can generate independent communication rates. It operates as a serial-parallel parallel-serial converter.

It manages both asynchronous and synchronous serial communications.

In asynchronous mode, the SCC can transmit characters containing from 5 to 8 bits. Users can program the basic clock division factor. The SCC can detect and generate BREAK signal and parity. Finally, the SCC can detect parity, overwrite and frame errors.

The SCC supports synchronous communication modes such as synchronous character mode (MONOSYNC, BISYNC) and synchronous bit mode (HDLC/SDLC).
In all these modes, the SCC can generate a CRC during transmission and can detect receive errors (CRC errors, frame errors, overwritten characters, parity errors).
The receive and transmit clocks used for synchronization may be external, internal, or may be extracted from data received.

Each channel on the SCC contains a programmable baud rate generator. The SCC's clock is first pre-divided (by 1 in synchronous mode, by 16 in asynchronous mode), then goes through a programmable divider. The transmit and receive clocks may be provided:

- either by the output of this divider,
- or from a pin on the line interface,
- or may be extracted from data received using sampling techniques (in this case the divider output must be 32 times faster than the expected rate).

SCC interrupts

The SCC features three types of interrupts:

* Receive interrupts.
* Transmit interrupts.
* Change of state interrupts.

Each of these types of interrupts is controlled by the user's program. Channel A has a higher priority than channel B. In each channel, the receiver has priority over the transmitter, which in turn has priority over the change of state interrupt.

When the transmit interrupt is enabled, the CPU receives an interrupt when the transmitter changes from the non-empty to the empty state. The transmitter must contain at least one character in order to trigger an interrupt.

When the receive interrupt is enabled, the CPU may be interrupted by any of these three methods:

* when the first character is received, or when a special condition is detected.
* when all characters are received, or when a special condition is detected.
* only when a special condition is detected.

The first two cases are the most often used when transferring blocks of data; the special condition is the detection of one or more of the following events:

* Receiver data is overwritten.
* Frame error.

Finally, the major function of the change of state interrupt is to alert the CPU when one of the following signals changes state:

* /CTS.
* /DCD.
* /RI (SYNC).
* BREAK/ABORT.

SCC Architecture

The SCC's internal structure features two independent "full duplex" channels, two baud rate generators, control and interrupt logic, and an interface for a non-multiplexed bus. Each channel has associated read and write registers. These registers control the SCC and provide status information on the unit. The logic for both channels "formats" the data and synchronizes and enables data transfer to and from the bus interface.

The state of the signals used to pilot modems is directly controlled by programming the control registers; all the modem signals are general-purpose signals which may, of course, be used for various applications.

The following registers are for both SCC channels:

* Write registers WR0 - WR15.
* Read register RR0 - RR3, RR10, RR12, RR13, RR15.

- **The read registers:**

NAME	Register usage
RR0	Status of TX, RX and external signals
RR1	Status of special conditions
RR2	Vector
RR3	Current interrupt
RR8	Receive buffer
RR10	Miscellaneous status bits
RR12	Least significant byte of the baud rate generator time constant
RR13	Most significant byte of the baud rate generator time constant
RR15	External interrupt status

- **The write registers:**

NAME	Register usage
WR0	Registers pointer, initialization conditions
WR1	TX, RX interrupt and transfer mode
WR2	Interrupt vector (accessible from both channels)
WR3	Parameters and control for reception
WR4	Auxiliary transmit and receive parameters
WR5	Parameters and control for transmission
WR6	Sync characters for MONOSYNC and BISYNC or SDLC address field
WR7	Sync characters for BISYNC or SDLC options
WR8	Transmit buffer
WR9	Interrupt control and reset
WR10	Miscellaneous synchronous control parameters
WR11	Clock control
WR12	Least significant byte of the baud rate generator time constant
WR13	Most significant byte of the baud rate generator time constant
WR14	Auxiliary controls
WR15	External interrupt control

Appendix E: RS422A-RS485 INTERFACE

RS422 and RS485 are electrical standards that provide for transmitting data in differential mode. This method provides noise immunity and enables long-distance transmission.

Notation for RS422A-RS485 signal status

VOLTAGE	NEGATIVE	POSITIVE
BINARY STATE	1	0
CONDITION	MARK	SPACE
FUNCTION	OFF	ON

RS422A-RS485 signal characteristics in idle state

EIA RS422A/485 - CCITT V11	
+TX A -TX B	A has a lower potential than B in the idle state (1, MARK or OFF)
+RX A' -RX B'	A' has a lower potential than B' in the idle state (1, MARK or OFF)

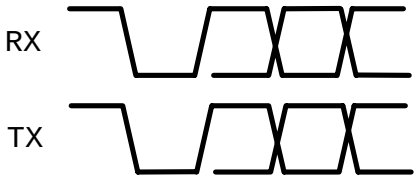
The +TX and +RX differential signals have a lower potential than the -TX and -RX signals in an idle state.

This remark is especially important when connecting to other RS422A-RS485 interfaces. Confusion reigns among many manufacturers concerning the naming of the +TX, +RX, -TX and -RX (A, A', B and B') signals.

RS422-RS485 SIGNAL TIMING DIAGRAM

FULL-DUPLEX

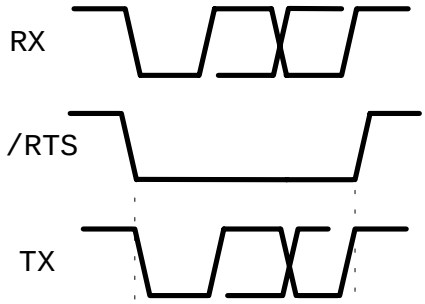
Permanent transmit enable



RS422A

FULL-DUPLEX

Controlled transmit enable

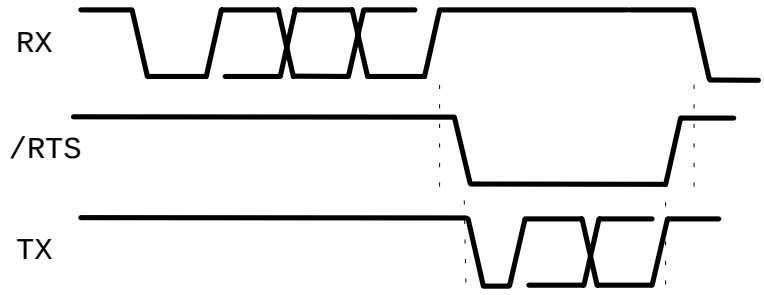


MULTIPOINT RS422A

RS485 2 pairs

HALF-DUPLEX

Controlled transmit enable



RS485

RS422A and RS485 transmission line characteristics

Terminating resistor:

The line terminating resistor for the receiver in RS422A mode (100Ω) and for the transceiver in RS485 mode (120Ω) help to reduce noise generated over long high-speed lines that disturbs reception.
The terminating resistor is not necessary in the following cases:

* Noise-free environment.
* Distances and rates between 1000m at 9600 bits/second and 100m at 112 K bits/second.

Polarization :

Line polarization is required for a stable state in the following cases:

* In RS485 mode, when switching from transmit to receive.

* In RS422A mode, if several transmitters are on the bus and, as a result, a high impedance state must be used.

Only one polarization is necessary per line.

Cable specifications:

* Twisted pair(s), may or may not be shielded, gauge 22-24 AWG, nominal impedance 100-120 Ω.

* Capacitance between conductors: 50 pF.

* Capacitance between shielding and conductors: 70 pF max.

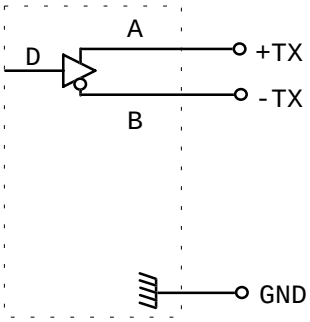
* Shielded cable is required in very noisy industrial environments; only ground one end of the cable.

* Connect the GND:
  - either by a wire shared by all the interfaces,
  - or by grounding each interface (use the same reference ground for all the equipment).

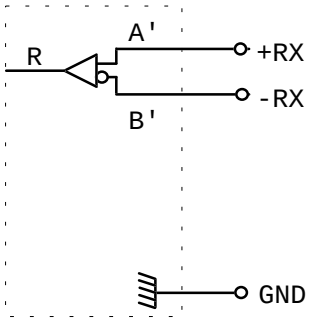
  If you use galvanically insulated interfaces, the GND connection is not mandatory. The voltage in common mode will be limited to the voltage of the galvanic insulation.

RS422A CONNECTION (4 WIRES)

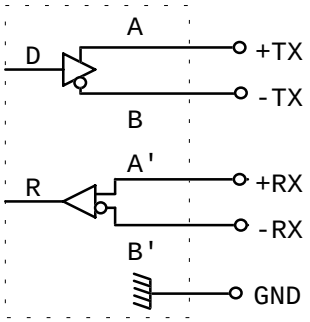
SIMPLEX
RS422A INTERFACE FOR POINT-TO-POINT OR MULTIPOINT
LINE - MASTER



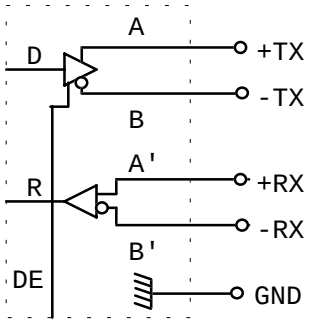
SIMPLEX
RS422A INTERFACE FOR POINT-TO-POINT OR MULTIPOINT
LINE - SLAVE



FULL-DUPLEX
RS422A INTERFACE FOR POINT-TO-POINT OR MULTIPOINT
LINE - MASTER

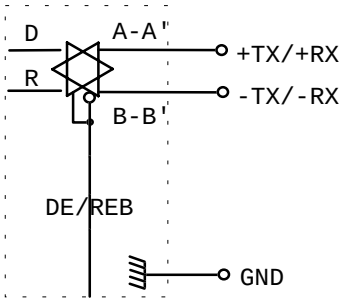


FULL-DUPLEX
RS422A INTERFACE FOR POINT-TO-POINT OR MULTIPOINT
LINE - MASTER/SLAVE (POLLING-SELECTING)

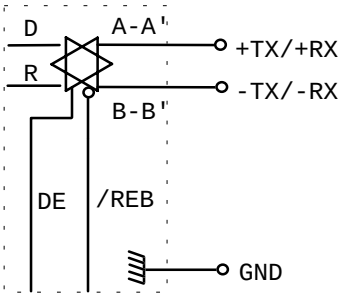


RS485 CONNECTION (2 WIRES)

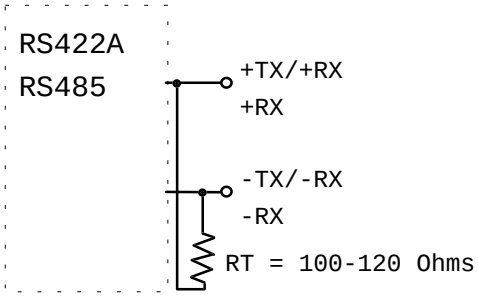
HALF-DUPLEX
RS485 INTERFACE FOR POINT-
TO-POINT OR MULTIPOINT LINE
MASTER/SLAVE (POLLING-SELECTING)



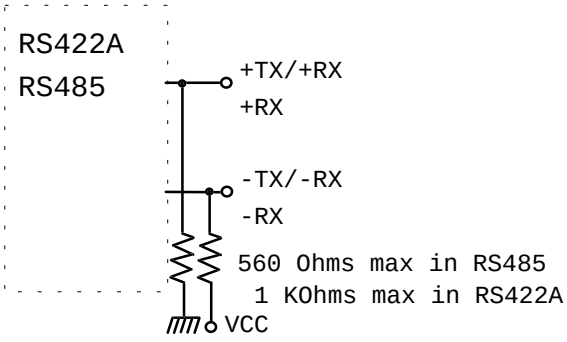
HALF-DUPLEX
RS485 INTERFACE FOR POINT-
TO-POINT OR MULTIPOINT LINE
MASTER/SLAVE (POLLING-SELECTING)



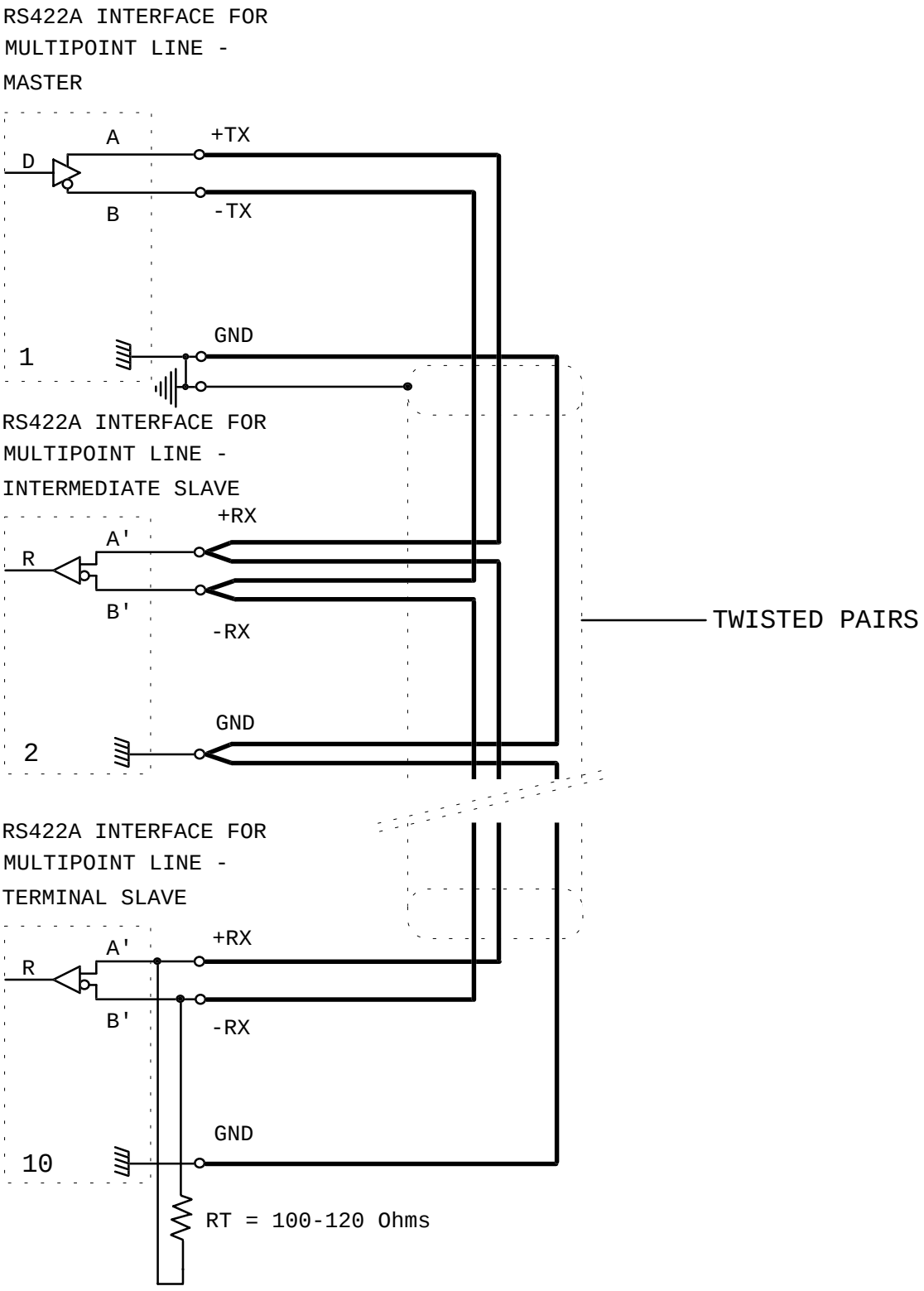
TERMINATING RESISTOR



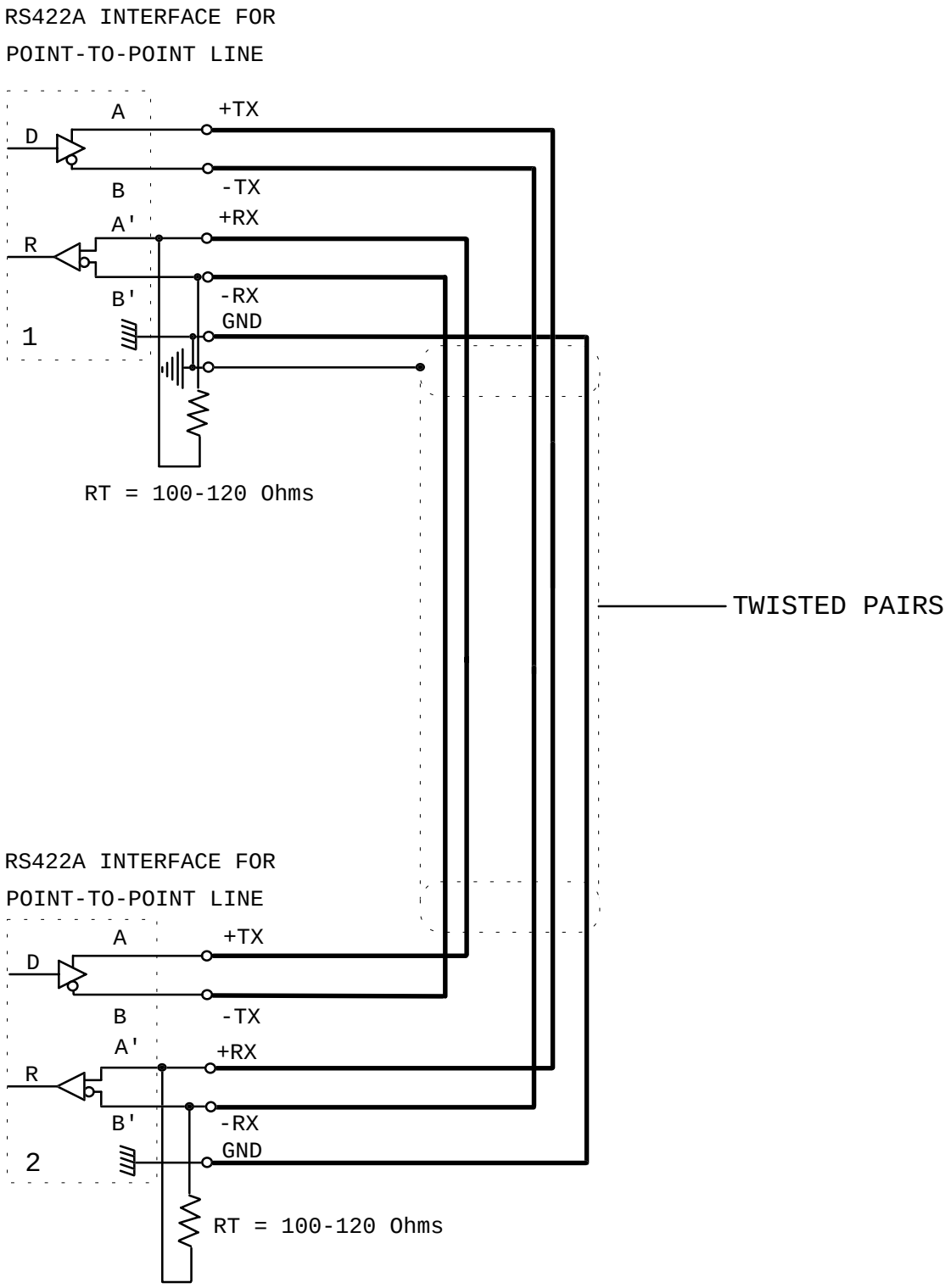
TERMINATING RESISTOR



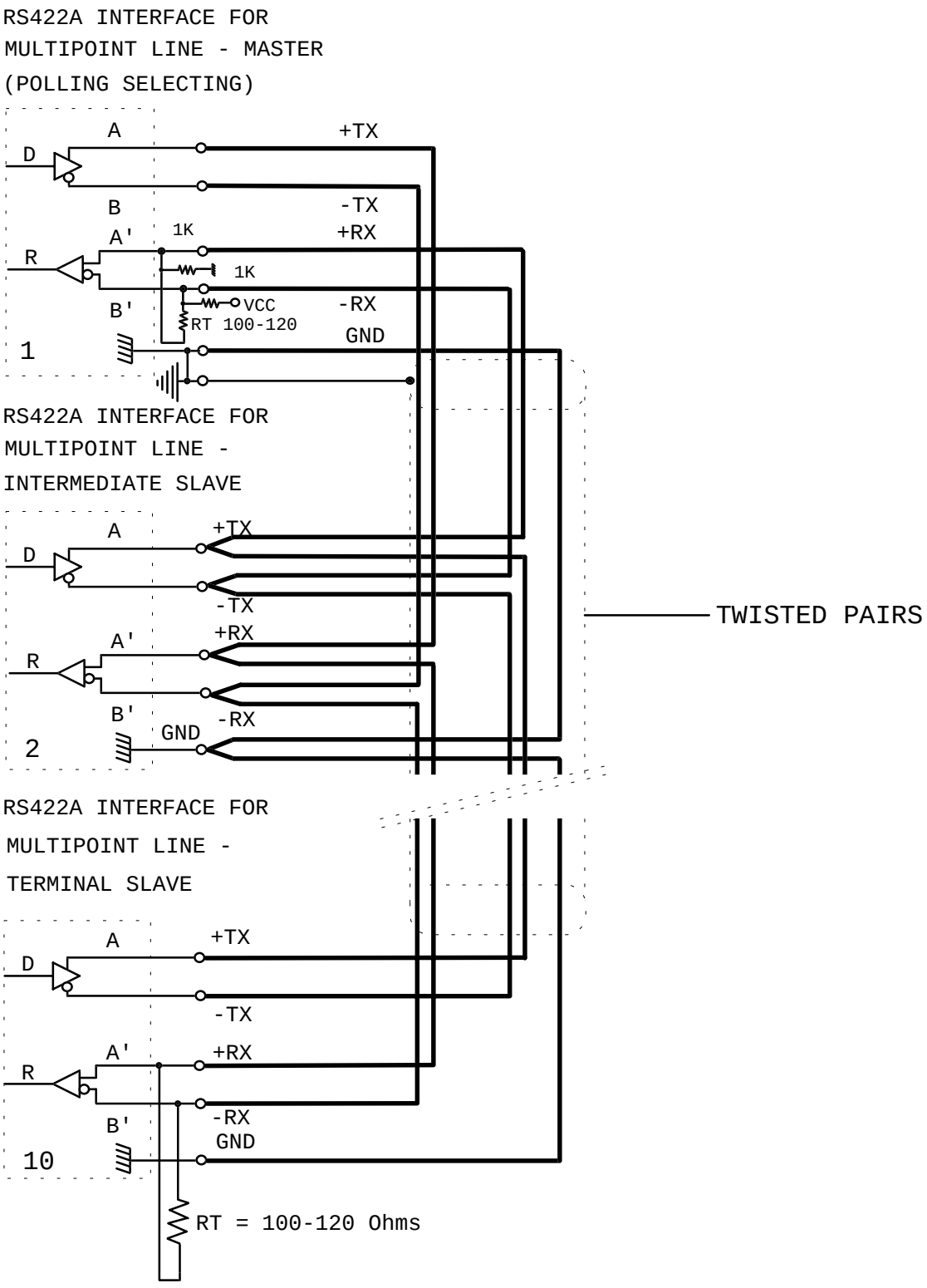
RS422A SIMPLEX MULTIPOINT CABLING



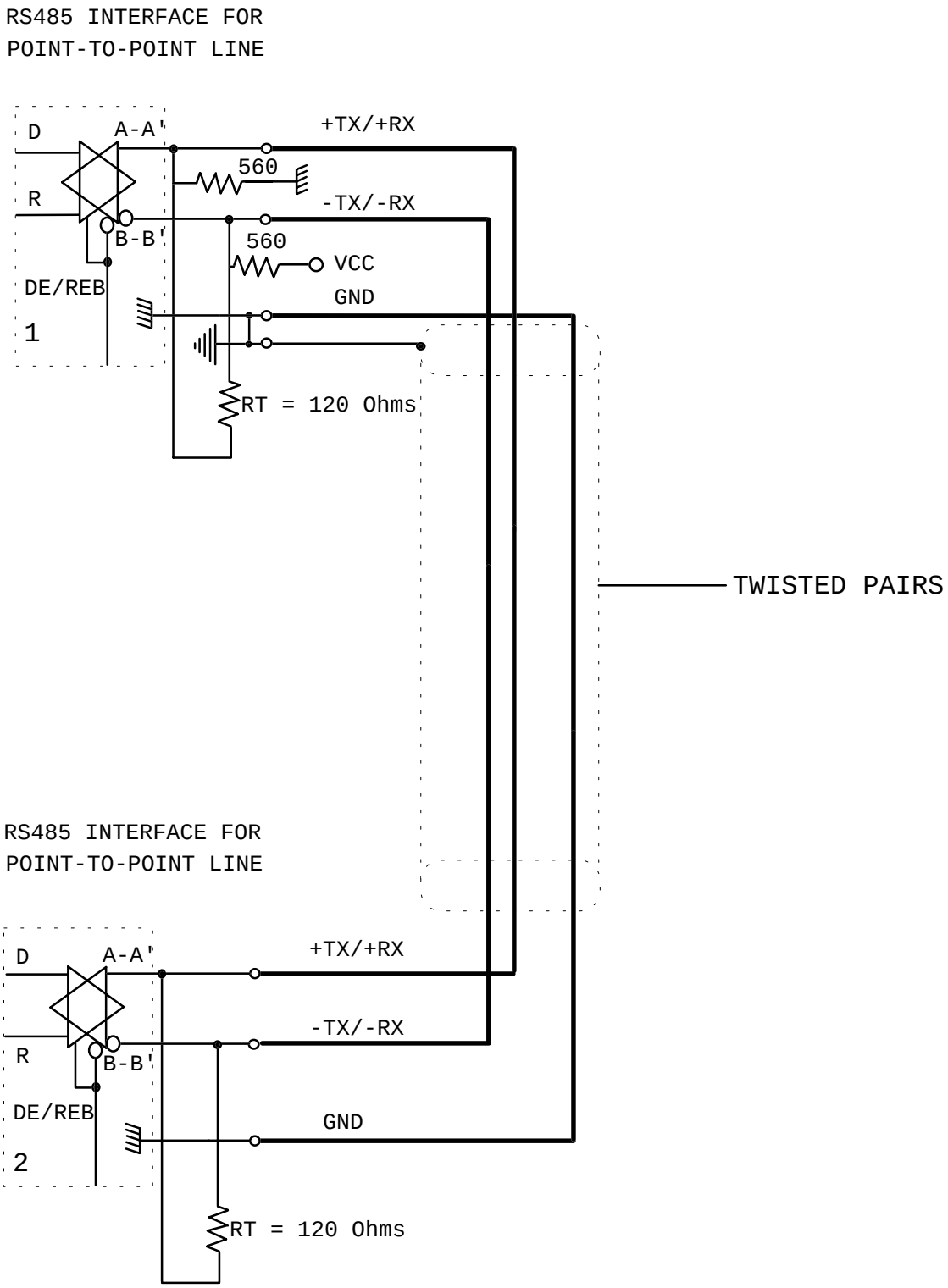
RS422A FULL-DUPLEX POINT-TO-POINT CABLING



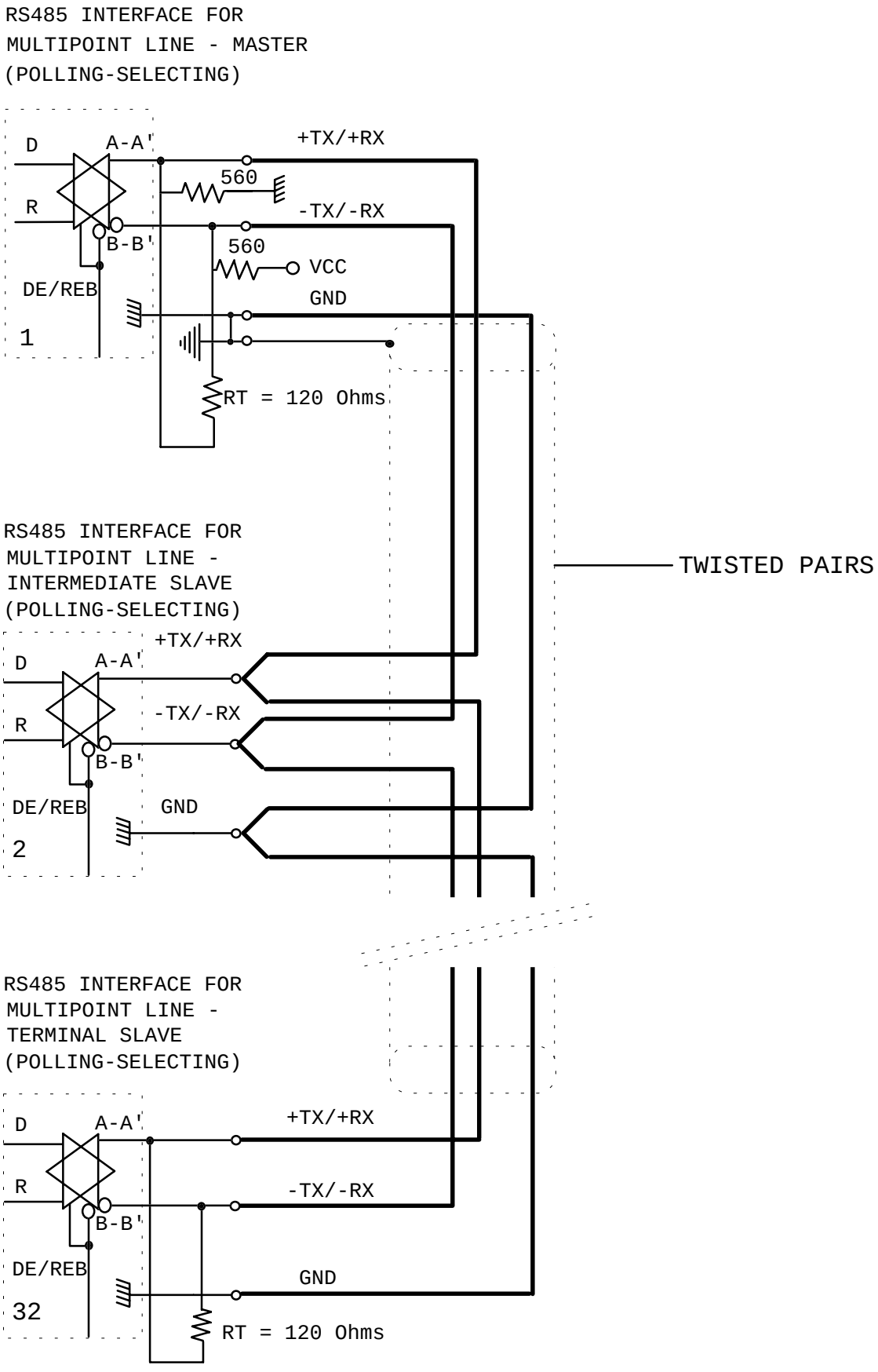
RS422A FULL-DUPLEX MULTIPOINT CABLING



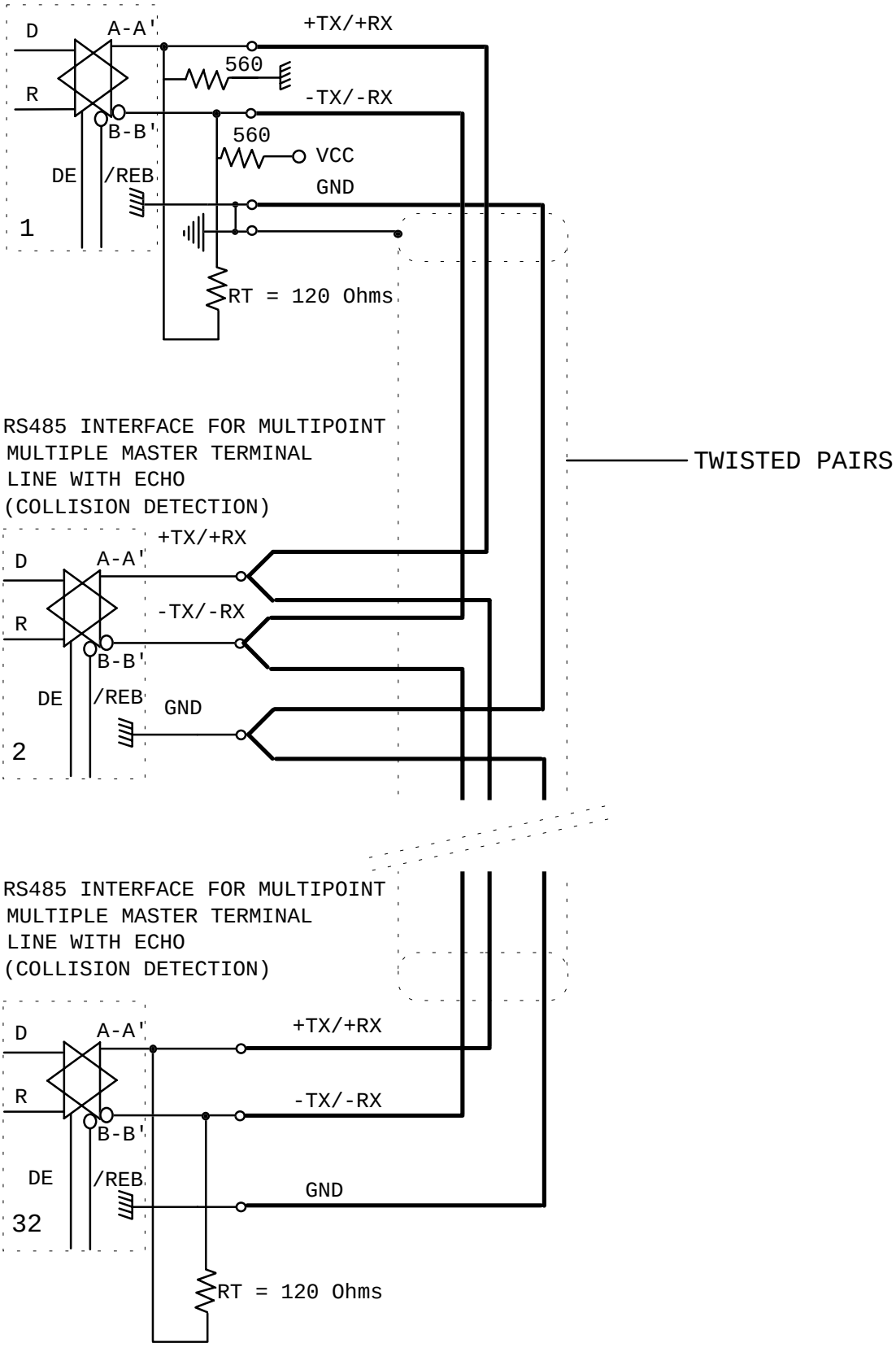
RS485 HALF-DUPLEX POINT-TO-POINT CABLING



RS485 HALF-DUPLEX MULTIPOINT CABLING

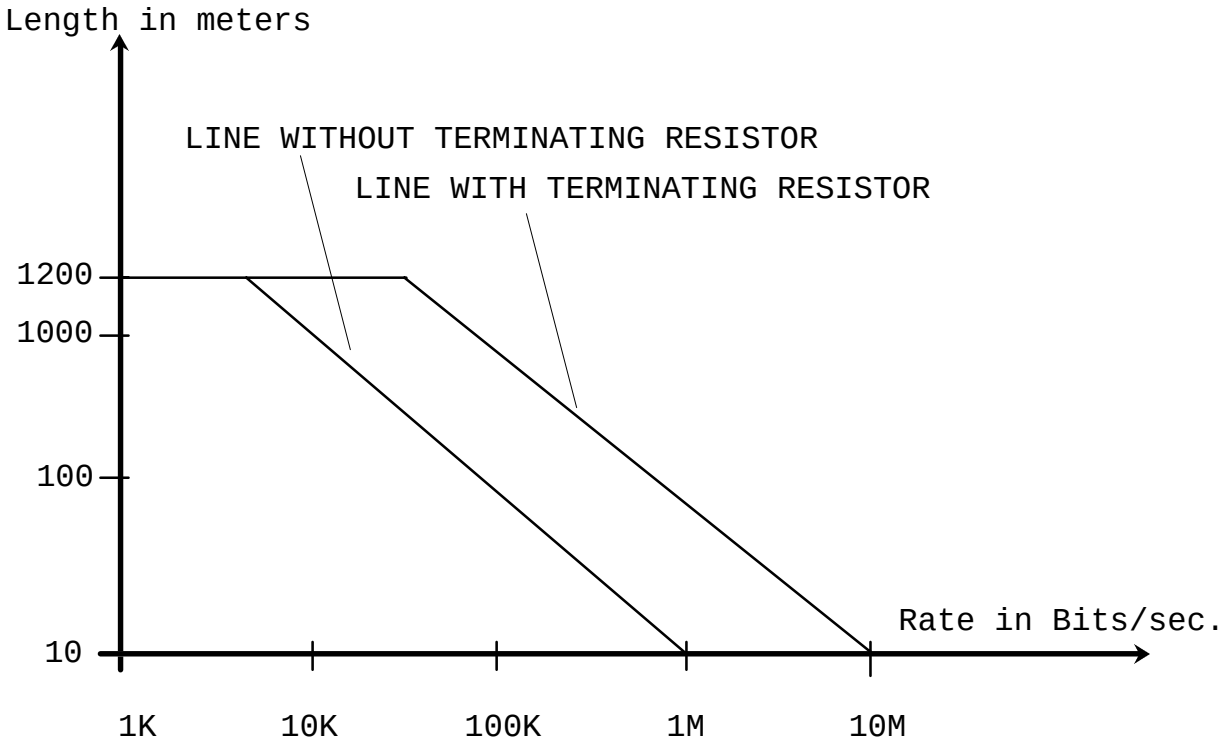


RS485 HALF-DUPLEX MULTIPOINT CABLING



CABLE LENGTH FOR RS422A OR RS485 LINES

Minimum values for a 24 gauge AWG twisted pair cable



Appendix F: ESD CHARACTERISTICS OF THE MCX CARDS

The cards in the MCX range receive exceptional protection against voltage surges and electrostatic discharges (ESD).

Each RS232D and RS422A signal is protected by devices which absorb voltage peaks that might damage electronic equipment.

Along with the shielded cable, this protection system makes the cards extremely reliable, extends their lifetime, reduces their electromagnetic interference and protects them from external parasites.

All these elements make the cards in this range ideal tools for communications applications in noisy industrial environments.

If the communications line are subject to large voltage surges or spikes (lightning, direct connection to a power supply, etc.) the protective devices self-destruct in order to protect the card and the host system.

Extracts from an ESD test report

These tests were carried out following the CEI 801-2 and MIL STD 883C 3015-X method standards; the severity of these tests exceeded the highest levels specified by the standards.

The following table summarizes the results obtained from applying electrostatic discharges directly to the RS232D signals. These tests were carried out during the execution of a test program by connecting the output signals to the input signals:

MINIMUM ESD VOLTAGES DISTURBING THE OUTPUT SIGNALS				
ACKSYS Cards	Isolated discharges	12 sequential discharges	20Hz bursts over 1 second	20Hz bursts over 5 seconds
MCX	16 kV	8 kV	14 kV	7 kV
MCX-*Lite*/S	16 kV	8 kV	14 kV	7 kV
MCX-*Lite*/U	9 kV	7 kV	7 kV	7 kV
MINIMUM ESD VOLTAGES APPLIED TO OUTPUT SIGNALS THAT GENERATE SEMI-PERMANENT OR PERMANENT DISRUPTIONS				
MCX	17 kV	14 kV	14 kV	12 kV
MCX-*Lite*/S	17 kV	14 kV	14 kV	12 kV
MCX-*Lite*/U	14 kV	8 kV	8 kV	8 kV

No functional disruptions nor any damage was noticed during the ESD tests when charges up to 25 kV[1] +/- 10% were applied to the units' metallic housing (which represent the limits of the generator).

The full of the ESD test report is available upon request.

[1] 22kV for the MCX-*Lite*/U card.

Appendix G: EXCERPTS FROM THE EIA STANDARD

The table below presents the various characteristics of the EIA/TIA-562 (RS232, EIA/TIA-574, EIA/TIA-561, etc.), RS422A and RS485 standards.

This chart is particularly useful for maximum authorized cable lengths for the various standards.

SPECIFICATIONS		EIA/TIA-562 (RS232 ...)	RS-422A	RS-485
Type of communications		Unipolar	Differential	Differential
Number of transmitters and receivers allocated per line		1 transmitter 1 receiver	1 transmitter 10 receivers	32 transmitters 32 receivers
Maximum cable length		16.5 m.	1320 m.	1320 m.
Maximum rate		64 Kbits/sec.	10 Mbits/sec (over 13 m)	10 Mbits/sec (over 13 m)
Voltage in shared mode on transmitter		±25V	±7V	-7V to +12V
Transmitter voltage level	Loaded	±5V	±2V	±1.5V
	Empty	±15V	±5V	±5V
Load resistance on the transmitter		3 to 7 KΩ	100Ω	54Ω
Transmitter leakage current	Powered on	.....	.....	±100µA
	Powered off	V_{max}/300Ω	±100µA	±100µA
Transition time		30V/µS max	.....	.....
Voltage range at receiver input		±15V	-7V to +7V	-7V to +12V
Receiver sensitivity		±3V	±200mV	±200mV
Resistance of receiver input		3 to 7 KΩ	4 KΩ min.	12 KΩ min.

Appendix H: ELECTROMAGNETIC COMPATIBILITY (EMC)

This equipment generates and uses electromagnetic frequencies and, if it is not installed and used strictly according to the manufacturer's specifications, it may generate interference which disturbs television and radio reception.

This digital device does not emit any electromagnetic noise exceeding the limits for a Class A digital device, as specified in section J.15 of the "FCC Rules and Regulations" concerning electromagnetic interference.

If this equipment nevertheless produces radio or television interference, we suggest you may remove this interference by following one or more of the measures below:

- Change the orientation of the antenna.
- Move your computer away from the antenna.
- Plug your computer into a different wall socket from your tuner.

Contact ACKSYS or an experienced RADIO-TELEVISION technician for further suggestions are necessary.

Appendix I: NOTES

Appendix J: EVALUATION SHEET

We appreciate your comments and suggestions for improving the quality and ease of use of our documentation.

We would be grateful if you could take a few moments to fill out this evaluation sheet and return it to us.

Thanks in advance.

COMPANY:	Telephone:
User:	Position:
Address:	
Zip Code:	City:
	Country:

Clearly indicate the version of the card, the software and the documentation:

• MCX Card	
• MCX-*Lite*/S Card	
• MCX-*Lite*/U Card	
• MCX-*Lite*/485 Card	
• MCX-*Lite*/104 Card	
• FLASH EPROM Revision	
• Documentation Revision	

Please give a grade from 0 (worst) to 10 (best) for each of the following characteristics:

Format	☐	Presentation	☐	Organization	☐
Clear	☐	Precise	☐	Explanations	☐

Errors:

If you find any errors in this document, please note the page number and describe the type of error, or write the modifications on the pages in question and send photocopies of those pages along with this report.

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